Learning Objectives:

At the end of this topic you will be able to;

☑ recognise, analyse and design circuits containing D-type flip-flops to form parallel-in-serial-out (PISO) registers, and serial-in-parallel-out (SIPO) registers;
☑ draw timing diagrams.
Shift Registers

In Module ET1 we introduced the D-Type Flip Flop and demonstrated how it could be used as a counter. In this topic we will develop another application of the D-Type Flip-Flop, that is the shift register.

A shift register is a very important functional unit in modern digital systems, as it is used for helping to move data from one system to another. More importantly it is able to swap data transfer from serial to parallel, or parallel to serial. This will be extremely important when we meet our next topic 4.5.4 - Pulse Code Modulation, however for now we will focus just on the operation of the shift register. First we will look at the two types of communication, just to refresh your memory,

Serial Transfer:

In serial transfer, data is moved along a single data line from one location to another, one bit at a time, the process can be slow, but only has to carry one signal along one pair of wires in the connecting cable, and therefore is very economical to make.

Parallel Transfer:

In parallel data transfer, the data is moved along multiple data paths at the same time, in the case shown above, 8 bits are moved at the same time. Data transfer is quick, but the cable has to be able to carry 8 signals along 8 pairs of wires in the cable at the same time and is therefore much more expensive than serial transfer.
Note: Advances in modern techniques now enable serial communication links to operate at near the same rate as parallel links. e.g. modern USB2 Serial links operate at very high speeds, giving the data transfer rate of a parallel link in serial form.

The shift register is a functional unit which acts as an interface to allow data to be transferred from a serial to parallel or from parallel to serial systems.

We will now look at how these interfaces can be constructed from D-Type Flip Flops. The first type we will look at is the Serial-In-Parallel-Out (SIPO). The circuit required is as follows:

At first glance you might think that this is the circuit for a counter, and indeed in examinations a significant number of candidates think it is and draw timing diagrams suitable for a counter, quite incorrectly of course!

There are a couple of observations to be made about this circuit which clearly separate it from the counter circuits encountered in ET1

i. The clock signal is common to each D-Type, so they are all clocked at the same time.
ii. The Q-output of each D-Type is connected to the D-input of the next flip-flop in the chain.
iii. The Q̅-output of each D-Type is not connected.

Looking out for these three characteristics should help you to distinguish the shift register from the counter.
This type of shift register takes in serial data through the \( D_{IN} \) terminal, and parallel data is available at Output A, B, C and D. Other control circuitry which is not shown ensure that the correct number of clock pulses are received to transfer the data in and out of the shift register. In this particular case there are 4 clock pulses required to transfer four bits of data from the serial input to the parallel outputs. Larger shift registers are available and can be made quite easily just by linking more D-Type flip-flops into the chain.

We usually encounter four types of question related to Shift registers.

1. Registers connected via logic gates to other registers.
2. Drawing timing diagrams for shift registers.
3. Completing tables to show the status of self filling shift registers.
4. Complete a diagram to show how a SIPO shift register is connected, from a block diagram of un-connected D-Type flip-flops.
1. If we consider the first case, this is probably the most straightforward. You will be presented with a diagram similar to the one shown below.

Complete the diagram below to show the content of the registers after 4 clock pulses.

Registers A and B are straightforward, as these will fill with Logic 1 and Logic 0, respectively. You will need to remember your logic gates from ET1 to complete the output register. You should remember that the NOR gate gives an output of logic 1 when both inputs are at logic 0. The final diagram therefore becomes:
2. Now we will look at how to construct a timing diagram for the shift register. We are usually presented with a diagram similar to the one below to start.

At first it might appear a little daunting as how to proceed with the completion of such a large number of diagrams. The trick is to focus initially on the output for $Q_A$. You should remember from ET1 that the logic level of $D_{IN}$ is transferred to the $Q$ output on the rising edge of the clock pulse.
Note that all of the outputs have been reset to Logic 0. If we only consider the output $Q_A$, to start with, the output for the given $D_{IN}$ signal will be as shown below.
Now that the first output has been completed, the remaining outputs will be quite easy to complete, since $Q_A$ becomes the input for $D_B$, and will be transferred to $Q_B$ at the next clock pulse.
The remaining outputs are completed in the same way, since $Q_B$ becomes the input for $D_C$, and will be transferred to $Q_C$ at the next clock pulse etc.

This completes the diagram, the outputs for $Q_B$, $Q_C$ and $Q_D$ follow on from each other, the most important output to obtain is $Q_A$, so great care should be taken completing this particular output.
3. The third way in which shift registers appear in questions is the self-filling register which uses a logic gate to use some of the register bits to generate the next input bit. This is illustrated below.

![Diagram of a self-filling register with logic gates and flip-flops]

The counter is initially reset, so that outputs A, B, C and D are all at logic 0. Complete the following table to show the output for successive clock pulses.

<table>
<thead>
<tr>
<th>Clock Pulse</th>
<th>Outputs</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 0 0 0</td>
<td>Outputs are reset, output of logic gate is logic 1, since A and B are logic 0.</td>
</tr>
<tr>
<td>1</td>
<td>1 0 0 0</td>
<td>Output A becomes logic 1, as output of logic gate is moved into the shift register. The output of the logic gate now becomes logic 0, as it has a logic 1 and logic 0 at the input.</td>
</tr>
<tr>
<td>2</td>
<td>0 1 0 0</td>
<td>Output B becomes logic 1, picking up the output from A, whilst A becomes logic 0, as the output of the logic gate is a zero. The output of the logic gate remains logic 0, as it has a logic 0 and logic 1 at the input.</td>
</tr>
<tr>
<td>3</td>
<td>0 0 1 0</td>
<td>Output C becomes logic 1, picking up the output from B, whilst A becomes logic 0, as the output of the logic gate is a zero. The output of the logic gate now changes to logic 1, as it has two logic 0 inputs.</td>
</tr>
<tr>
<td>4</td>
<td>1 0 0 1</td>
<td>Output D becomes logic 1, picking up the output from C, whilst A becomes logic 1, as the output of the logic gate is a logic 1. The output of the logic gate changes to logic 0, as it now has a logic 0 and logic 1 at the input.</td>
</tr>
<tr>
<td>5</td>
<td>0 1 0 0</td>
<td>Output B becomes logic 1, picking up the output from A, whilst A becomes logic 0, as the output of the logic gate is a zero. The output of the logic gate remains logic 0, as it has a logic 0 and logic 1 at the input. The logic 1 at D is lost out of the register and the sequence repeats</td>
</tr>
<tr>
<td>6</td>
<td>0 0 1 0</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>1 0 0 1</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>0 1 0 0</td>
<td>etc</td>
</tr>
</tbody>
</table>

In this case the clock sequence was consecutive, however in an exam some steps may be left out. You will see an example of this in the student exercise.
4. The final type of question would be to complete a circuit diagram for a SIPO shift register from a basic block diagram as shown below. You will be given a circuit like this:

The diagram needs to be completed by adding the connections shown by the red lines below:

This completes our examination of the SIPO, and we will now turn our attention to the Parallel-In-Series-Out, PISO shift register. Examples of the SIPO will be found in Student Exercise 1 at the end of the topic.
Parallel-In-Serial-Out Shift Register

The basic layout of the PISO shift register is very similar to that of the SIPO, and care must be taken to ensure that you do not get the two mixed up. There are a number of different versions of the PISO circuit but for the purposes of this course the only one that will be used is as shown below.

The process of loading the register with data is as follows.

i. When first switched on the D-types are reset by pulsing the reset line to reset the output of all the D-types to logic 0.
ii. The data is then put on the data lines D₃, D₂, D₁, and D₀.
iii. The 'load' line is then taken to logic 1, which allows any logic 1, present on the D₃, D₂, D₁, and D₀ lines to SET the output of the corresponding D-Type to a logic 1. The load line is then taken back to Logic 0.
iv. The clock line then pulses four times to move the data out of the shift register.
v. As Dᵢ₅ of the first D-Type is connected to logic 0, there will be no need to reset the D-Types at the end of the 4 clock pulses as all D-Types will contain logic 0, ready for the next time data is loaded into the register.
Questions about the PISO shift register will be related to the following:

1. Complete a timing diagram for the shift register.

2. Complete an un-connected diagram of D-type flip-flops to make a PISO.

We fill first consider the possibility of completing a timing diagram for the PISO.

We start with a circuit diagram giving the logic levels of the parallel input data.

The timing diagrams applied to the Reset, Load, and Clock are shown on the following page. Complete the timing diagrams for \( Q_A, Q_B, Q_C, \) and \( Q_D \).
This is the way in which the timing diagram would be presented in the examination. We will now consider stage by stage what happens as the signals are applied. Note that $Q_A$, $Q_B$, $Q_C$, and $Q_D$, have been given some initial value.
The first signal to have any effect on the outputs of $Q_A$, $Q_B$, $Q_C$, and $Q_D$ will be the reset pulse which will reset all outputs to logic 0, as shown below.
Next will be the effect of the 'Load' signal, which will set the outputs to the state of the parallel inputs, as shown in the original circuit diagram, as shown below.
The data has now been loaded into the Shift register, so now the clock pulses take over to move the data through, the register. The input to the register is set to logic 0 so this keeps moving in logic 0 at the input with every clock pulse. After one clock pulse we have.
At the next clock pulse these diagrams will look like the following:
And then after clock pulse 3, the graph would look like this.
If the inputs have been left unchanged from the circuit diagram, then the timing diagram would be completed as follows:

![Timing Diagram](image-url)
The data has now been shifted out of the register and all outputs have been set to logic 0, ready for the next parallel load pulse.

Notice that four clock pulses are required to empty the register and ensure that all bits are set to logic 0 prior to the 'load' line going high to enter the next four bits of data into the register.

The completion of the timing diagram is a little more involved than a SIPO and care should be taken when drawing this type of diagram. The control circuitry used to synchronise the reset, load and clock signals is complex and is not covered in this syllabus.

The second type of question for the PISO is to complete the drawing of the circuit as shown on page 13. You will find an example of this in the following student exercise which will include questions on both SIPO and PISO shift registers.

Student Exercise 1.

1. Complete the circuit diagram below to make a 4-bit Serial-In-Parallel-Out shift register. Label the outputs A, B, C and D.
2. The following diagram shows three shift registers. Complete the output register to show the contents after four clock pulses to the shift registers.

```
Register A
0 → 1 0 0 1

Register B
0 → 1 0 1 0
```

Output Register

3. Complete the following diagram to show how the four D-Type flip-flops can be connected with some logic gates to form a 4-bit Parallel-In-Serial-Out shift register.

Parallel Input

```
| D_3 | D_2 | D_1 | D_0 |
```

Load

Logic 0

Reset

Clock

--- Serial Output
4. The following circuit shows a SIPO shift register which uses a logic gate to use some of the register bits to generate the next input bit.

The counter is initially reset, so that outputs A, B, C and D are all at logic 0. Complete the following table to show the output after the number of clock pulses shown.

<table>
<thead>
<tr>
<th>Clock Pulse</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>
5. The circuit diagram below shows a 4-bit SIPO shift register.

![SIPO Shift Register Diagram]

Complete the timing diagram opposite for $Q_A$, $Q_B$, $Q_C$, and $Q_D$, for the clock and Data In signal shown.
Topic 4.5.3 – Shift Registers

Clock

D_in

Q_A

Q_B

Q_C

Q_D

WJEC

CBAC
6. A 4-bit Parallel-In-Serial-Out shift register is shown below.

![Parallel-In-Serial-Out Shift Register Diagram]

Complete the timing diagrams opposite to show how the outputs change in relation to the applied signals.
Topic 4.5.3 – Shift Registers

- Reset
- Load
- Clock
- Q_A
- Q_B
- Q_C
- Q_D
Module ET4 – Communication Systems

Solutions to Student Exercise.

Student Exercise 1.

1.

![Diagram of digital circuits](image)

2.

![Diagram of registers](image)
3.

Parallel Input

Load

Logic 0

Reset

Clock

Serial Output

4.

<table>
<thead>
<tr>
<th>Clock Pulse</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A  B  C  D</td>
</tr>
<tr>
<td>0</td>
<td>0  0  0  0</td>
</tr>
<tr>
<td>1</td>
<td>1  0  0  0</td>
</tr>
<tr>
<td>2</td>
<td>0  1  0  0</td>
</tr>
<tr>
<td>3</td>
<td>1  0  1  0</td>
</tr>
<tr>
<td>4</td>
<td>1  1  0  0</td>
</tr>
<tr>
<td></td>
<td>0  1  1  0</td>
</tr>
<tr>
<td></td>
<td>0  0  1  1</td>
</tr>
<tr>
<td>7</td>
<td>0  0  0  1</td>
</tr>
<tr>
<td></td>
<td>1  0  0  0</td>
</tr>
<tr>
<td></td>
<td>0  1  0  0</td>
</tr>
<tr>
<td>10</td>
<td>1  0  1  0</td>
</tr>
</tbody>
</table>
Now for some practice examination questions.
Examination Style Questions.

1. a. How many clock pulses does it take to load a 4-bit number into
   i) a 4-bit PISO (parallel-in-serial-out) shift register?

   .................................................................  [1]

   ii) a 4-bit SIPO (serial-in-parallel-out) shift register?

   .................................................................  [1]

   b. Complete the following circuit diagram for a SIPO shift register, that uses four D-Type
   flip-flops. Label the serial input and one of the parallel outputs.

   ![Circuit Diagram]

   [4]
The following circuit diagram shows a SIPO shift register with outputs A and B connected to a NOR gate. The output of the NOR gate is used to generate $D_{IN}$.

The shift register is reset so that outputs A, B, C and D, are logic 0. Complete the following table to give the state of the output after the given number of clock pulses have been applied.

<table>
<thead>
<tr>
<th>Clock Pulse</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
</tr>
</tbody>
</table>
3. The following circuit diagram shows a SIPO shift register with outputs A and C connected to a NOR gate. The output of the NOR gate is used to generate $D_{IN}$.

The shift register is reset so that outputs A, B, C and D, are logic 0. Complete the following table to give the state of the output after the given number of clock pulses have been applied.

<table>
<thead>
<tr>
<th>Clock Pulse</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>

4. The circuit diagram shows a three bit shift register, made from rising-edge-triggered D-type flip-flops.
Initially all three flip flops are reset.

The upper two graphs shows the signals applied to the data input and clock input. Use the axes provided to show the corresponding signals at the outputs A, B and C.
5. The following diagram shows a 4-bit Serial-In-Parallel-Out shift register, made from rising edge triggered D-type flip-flops.

Using the axes below, draw the output observed on the outputs A, B, C, and D during the period shown. Assume all outputs are initially at logic 0.
6. The diagram shows 3-D-Type flip-flops that are rising edge triggered.

(a) Complete the diagram to show how these are connected to make a 3-bit Serial-In-Parallel-Out (SIPO) shift register, with a reset facility.

(b) Initially all three flip-flops are reset.

The first two graphs show the signal applied to the data input and clock input.

Use the axes provided to show the corresponding signals at the outputs A, B, and C.
7. A 4-bit Parallel-In-Serial-Out shift register is shown below.

Complete the timing diagrams opposite to show how the outputs change in relation to the applied signals.
Topic 4.5.3 - Shift Registers

![Diagram of shift registers with waveforms for Reset, Load, Clock, Q_A, Q_B, Q_C, Q_D]
8. The following circuit diagram shows a SIPO shift register with outputs A and C connected to a NAND gate. The output of the NAND gate is used to generate $D_{\text{IN}}$.

The shift register is reset so that outputs A, B, C and D, are logic 0. Complete the following table to give the state of the output after the given number of clock pulses have been applied.

<table>
<thead>
<tr>
<th>Clock Pulse</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>
9. The following diagram shows three shift registers.

(i) What is the name of the logic gate? .......................................

(ii) Complete the truth table for the logic gate.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

(iii) Complete the diagram below to show the contents of the registers after they have been clocked four times.

[3]
## Self Evaluation Review

<table>
<thead>
<tr>
<th>Learning Objectives</th>
<th>My personal review of these objectives:</th>
</tr>
</thead>
<tbody>
<tr>
<td>recognise, analyse and design circuits containing D-type flip-flops to form parallel-in-serial-out (PISO) registers, and serial-in-parallel-out (SIPO) registers;</td>
<td>☑ ☐ ☐</td>
</tr>
<tr>
<td>draw timing diagrams.</td>
<td>☑ ☐ ☐</td>
</tr>
</tbody>
</table>

**Targets:**

1. ..................................................................................................................................................
   ..................................................................................................................................................

2. ..................................................................................................................................................
   ...................................................................................................................................................