

Learning Objectives:

At the end of this topic you will be able to;

- Analyse and design a DAC based on an op-amp summing amplifier to meet a given specification.

Digital and Analogue Information

In many situations, real world information exists in analogue form, not digital.

Sensors may be monitoring temperature, or light intensity, or humidity, and outputting analogue signals such as voltages that increase as temperature / light level etc increase.

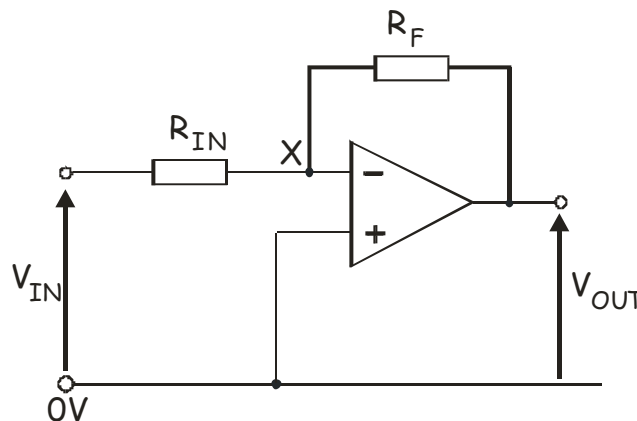
Output devices, such as motors, may rotate faster or slower, rather than being simply on or off. Sounders may be louder or quieter. Lamps can be brighter or darker. All of these require analogue signal processing.

PIC microcontrollers are digital devices. They process data in digital form, and so we often need to convert information from analogue sensors into digital data, process it with a PIC microcontroller, and then convert the digital output to an analogue signal again. The first of these operations requires an Analogue to Digital Converter (ADC). The second requires a Digital to Analogue Converter (DAC). This section looks at the second of these devices.

Digital to Analogue Converters

A DAC must generate an analogue output voltage which increases in size as the binary number applied to the input increases in size. There are a number of ways of achieving this. The approach used here modifies a summing amplifier circuit based on the op-amp inverting voltage amplifier.

ET1 section 1.4.2 covered the inverting voltage amplifier:



Voltage Gain G ($= V_{OUT} / V_{IN}$) = $- R_F / R_{IN}$
 (providing that the output is not saturated.)

The content of the following section is non-examinable!
It is aimed at improving your understanding of the summing amplifier.

The voltage gain formula relies on two properties of the inputs (inverting and non-inverting) of the op-amp.

1. **They both sit at the same voltage, unless the output saturates.**

In the inverting amplifier circuit, the non-inverting input is connected directly to the 0V power rail.

As a result, the inverting input and point X in the circuit diagram, also sit at 0V.

The voltage at the left-hand end of the input resistor $R_{IN} = V_{IN}$.

The voltage at the right-hand end of $R_{IN} = 0V$.

Hence:

- (a) the voltage drop across the $R_{IN} = V_{IN}$,
- and (b) the voltage drop across the feedback resistor $R_F = -V_{OUT}$.

(The minus sign takes into account the fact that this is an inverting amplifier - a positive input voltage produces a negative output voltage. Another way to view this is to look at the current flowing through the feedback resistor - see below.)

We next apply the Ohm's law formula to obtain expressions for the currents I_{IN} and I_F flowing through R_{IN} and R_F respectively:

$$I_{IN} = V_{IN} / R_{IN} , \text{ using (a)}$$

and

$$I_F = -V_{OUT} / R_F, \text{ using (b)}$$

2. They draw virtually no current.

The current flowing through the input resistor R_{IN} is identical to the current flowing through the feedback resistor R_F , (because the current flowing into the op-amp through the inverting input is so small that we can ignore it.)

In other words, $I_{IN} = I_F$

Combining these two sets of information:

$$I_{IN} = I_F$$

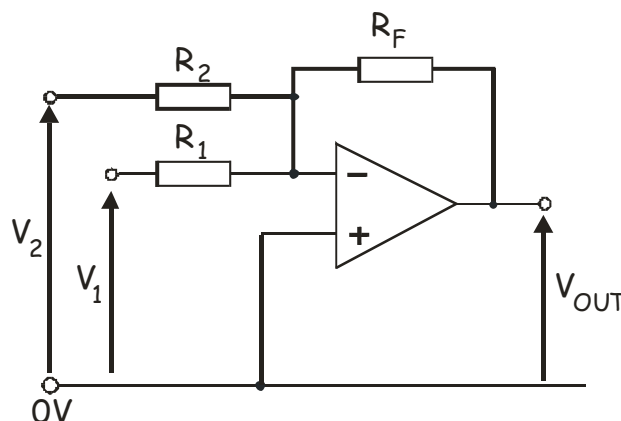
$$V_{IN} / R_{IN} = -V_{OUT} / R_F$$

Re-arranging this equation gives:

$$V_{OUT} / V_{IN} = - R_F / R_{IN}$$

This is the voltage gain formula quoted earlier!

The next step is to add a second input resistor, supplied with its own voltage signal. The labels have been changed so that the two input voltages can be identified separately. The new circuit diagram is:



Providing that the output is not saturated, the inverting input and the non-inverting input still sit at 0V.

The voltage drop across R_1 is still V_1 , and so the current flowing through R_1 is:

$$I_1 = V_1 / R_1$$

Similarly, the voltage drop across R_2 is V_2 and the current through it is:

$$I_2 = V_2 / R_2$$

As before, the current through the feedback resistor is:

$$I_F = -V_{OUT} / R_F$$

When we ignore the tiny currents flowing in the op-amp inputs we get:

$$I_F = I_1 + I_2$$

Substituting the values from the earlier equations:

$$-V_{OUT} / R_F = V_1 / R_1 + V_2 / R_2$$

This can be re-arranged to give :

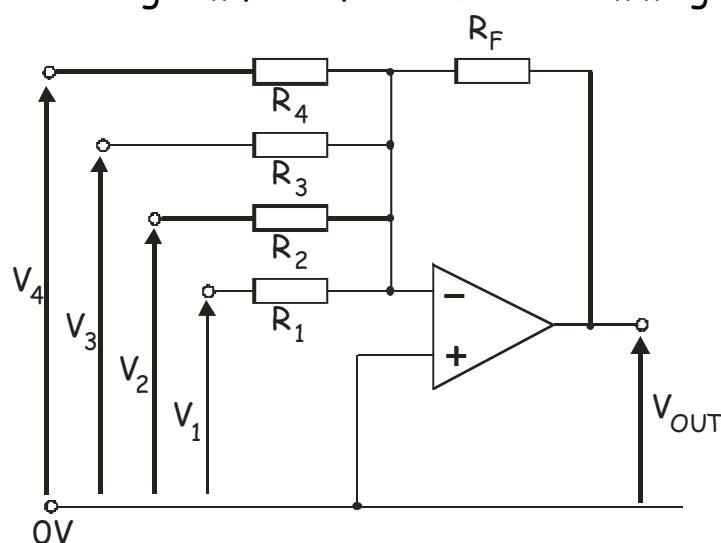
$$V_{OUT} = -R_F (V_1 / R_1 + V_2 / R_2)$$

This is the equation for the summing amplifier. Notice that it is the input currents that are summed as they flow through the feedback resistor.

In fact, the gain formula could be written, (but isn't!) as:

$$V_{OUT} = -R_F (I_1 + I_2)$$

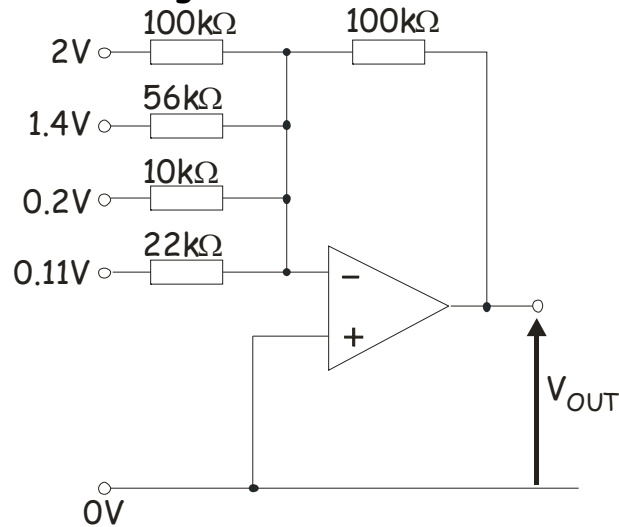
Further input signals can be added, each with its own input resistor, as shown in the following circuit diagram for a four channel summing amplifier:



The formula for this circuit is:

$$V_{OUT} = -R_F (V_1 / R_1 + V_2 / R_2 + V_3 / R_3 + V_4 / R_4)$$

For example, given the following circuit:



The output voltage will be:

$$V_{OUT} = -100 \left(\frac{2}{100} + \frac{1.4}{56} + \frac{0.2}{10} + \frac{0.11}{22} \right)$$

$$= -7V$$

Now back to the task in hand, the DAC, **and examinable content!**

Digital signals

A digital signal has two significant properties:

- It is a two state signal. It consists of a number of bits, each either logic 0 (~ 0V) or logic 1 (~+V_S).
- The place value of the bit (how much it is worth,) depends on its position.
 - The least significant bit (lsb) is worth either 0 (for logic 0) or 1 (for logic 1).
 - The next bit on the left is worth either 0 (for logic 0) or 2 (for logic 1).
 - The next is worth 0 or 4, and so on.

The table shows the value of a logic 1 signal in various positions in an eight bit binary number.

8 bit binary number								Decimal value
msb							lsb	
							1	1
						1		2
					1			4
				1				8
			1					16
		1						32
	1							64
1								128

Hence the binary number 10010011 is equivalent to the decimal number

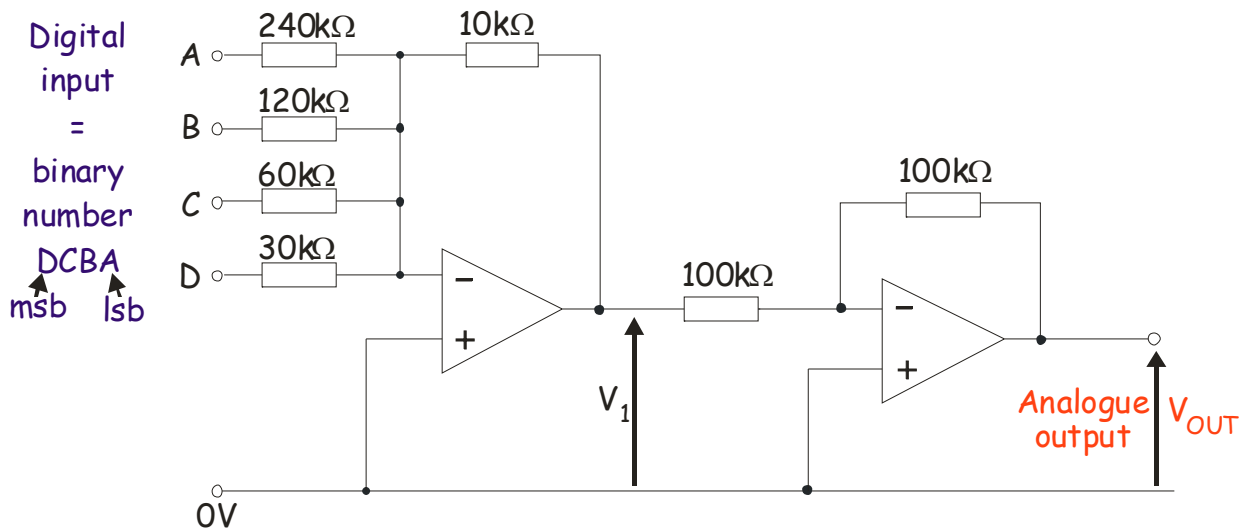
$$(128 + 16 + 2 + 1) = 147.$$

The DAC circuit must take into account both of these properties:

- The input voltages will be one of two values, either that representing logic 0, usually 0V, or that representing logic 1, usually close to the positive supply voltage ($+V_S$).
- The output voltage must take into account the place value of the logic 1 input signals, by having a voltage gain that reflects this place value. In other words, if the input receiving the least significant bit (lsb) has a voltage gain of G , then the input connected to the next bit must have a gain of $2G$, the next input a gain of $4G$, and so on. In DAC circuits based on the summing amplifier, this is achieved by successively reducing the size of the input resistor. When the lsb input resistor is R , the next input resistor will be $R/2$, the next $R/4$ and so on.

The design is based on an inverting amplifier, and so, when using positive logic (logic 1 = $+V_S$), the output voltage is negative. (The circuit must be powered from a split power supply, offering voltage rails at $+V_S$, 0V and $-V_S$.) To overcome the inversion, a second inverting amplifier often follows the first. This may simply have a voltage gain of -1.

The next circuit diagram shows these ideas incorporated into a 4 bit DAC:



Take care when choosing resistor values for this circuit!

It is very easy to saturate the output. The simplest way to avoid this is to use fractional voltage gains for the summing amplifier. In the above circuit, for example, the lsb (input A) has a voltage gain of 1/24, input B has a gain of 1/12, input C 1/6 and the msb, input D, a gain of 1/3.

Analysing a DAC circuit:

To analyse the above circuit, assume that 0V represents a logic 0 signal, and +12V a logic 1. Think of it as four inverting amplifiers combined so that the output voltage is the sum of their outputs. The second op-amp has a voltage gain of -1, and so simply reverses the polarity of the output signal.

For example:

- Input the binary number 0001,
i.e. A = 12V and B = C = D = 0V.

Voltage gain on A's input = $-R_F / R_{IN} = -10/240$,
so its output = $-12 \times 10/240 = -0.5V$.

The other inputs are set to 0V and so they output 0V.

The final output = $-(-0.5 + 0 + 0 + 0) = +0.5V$

- Input the binary number 1011,
i.e. $A = B = D = 12V$ and $C = 0V$.
Voltage gain on A's input = $-10/240$, and its output = $-12 \times 10/240 = -0.5V$.
Voltage gain on B's input = $-10/120$, and its output = $-12 \times 10/120 = -1.0V$.
Voltage gain on D's input = $-10/30$, and its output = $-12 \times 10/30 = -4.0V$.
The final output = $-(-0.5 + (-1.0) + 0 + (-4.0)) = +5.5V$

Exercise 1 (The solutions are given in the table that follows.)

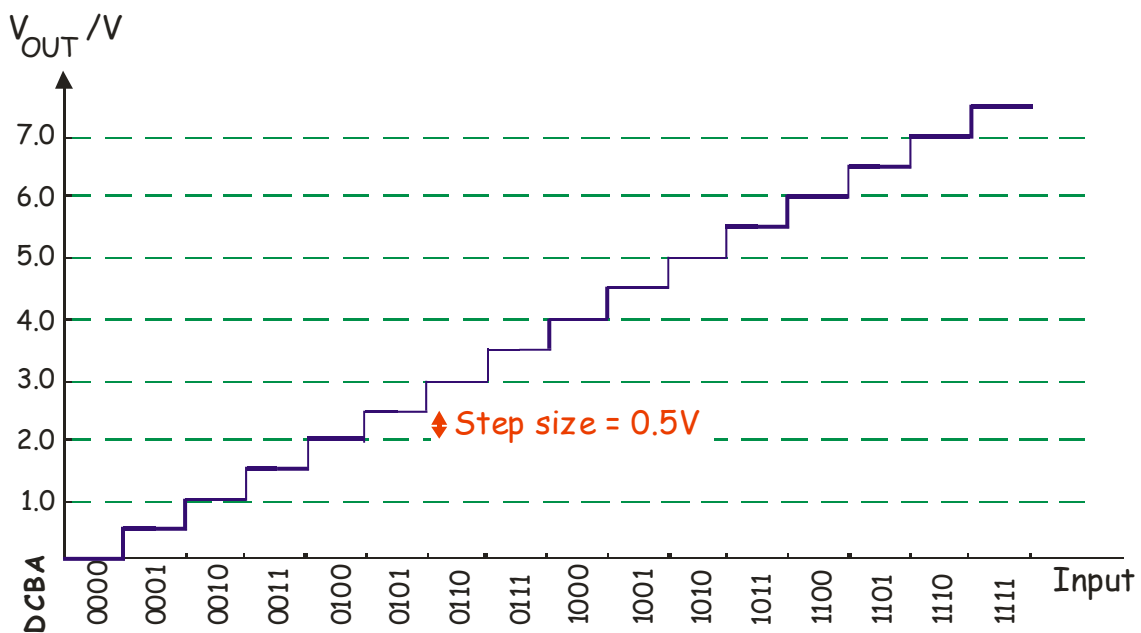
Calculate the output voltage V_{OUT} when the following binary numbers are applied to the input:

- (a) 0111
- (b) 1101
- (c) 1111

DAC output - summary

The behaviour of the four bit DAC can be summarised in two ways - as a table of output voltages, or as a graph. Both of these are shown below.

Binary number input				V_1 / V	V_{OUT} / V
D	C	B	A		
0	0	0	0	0	0
0	0	0	1	-0.5	0.5
0	0	1	0	-1.0	1.0
0	0	1	1	-1.5	1.5
0	1	0	0	-2.0	2.0
0	1	0	1	-2.5	2.5
0	1	1	0	-3.0	3.0
0	1	1	1	-3.5	3.5
1	0	0	0	-4.0	4.0
1	0	0	1	-4.5	4.5
1	0	1	0	-5.0	5.0
1	0	1	1	-5.5	5.5
1	1	0	0	-6.0	6.0
1	1	0	1	-6.5	6.5
1	1	1	0	-7.0	7.0
1	1	1	1	-7.5	7.5



Notice that the step size depends on the voltage gain of the least significant input of the DAC (and the voltage that represents logic 1.)

When viewed as a graph, the results show the characteristic staircase waveform. The output is analogue - it gets bigger as the digital input number gets bigger, but it is not continuous but rises in steps.

$$\text{Step size} = V_{L1} R_F / R_1$$

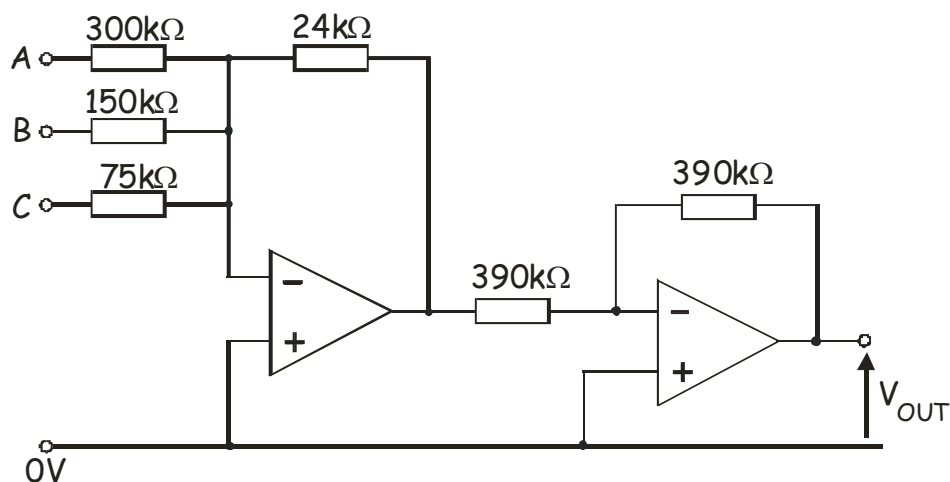
where V_{L1} = voltage corresponding to logic 1

R_F = feedback resistance

R_1 = input resistance for least significant input.

Exercise 2 (Solutions are given at the end of the topic.)

Here is the circuit diagram for a 3 bit DAC.



A logic 1 signal is represented by 10V and logic 0 by 0V.

Analyse the performance of this circuit by producing a table to show how the output voltage varies as increasing binary numbers are applied to the input.

Then plot these results as a graph of output voltage against input number.

Designing a DAC to meet a given specification:

The performance of the DAC can be described in a number of ways, including:

- the number of bits that can be inputted;
- the voltage range for the output;
- the step size for the output voltage;
- the speed of conversion;
- the power supply used.

For example, design a DAC with the following parameters:

- number of input bits = 4;
- output voltage range = 0 to 12V;
- logic 1 = 8V and logic 0 = 0V;
- power supply = +15V / 0V / -15V.

In general, a 'n' bit DAC will have 2^n output voltage levels, with $2^n - 1$ steps between them.

As can be seen on the graph on page 10, a four bit DAC produces sixteen ($=2^4$) output voltage levels, with fifteen 'steps' ($2^4 - 1$) between them.

These fifteen steps must cover the 0 to 12V voltage range, so that each step is a voltage change of $(12 / 15) V, = 0.8V$.

Using the formula quoted earlier:

$$\text{Step size} = V_{L1} R_F / R_1$$

where V_{L1} = voltage corresponding to logic 1 = 8V

R_F = feedback resistance

R_1 = input resistance for least significant input,

gives:

$$0.8 = 8 \times R_F / R_1$$

so that:

$$R_F / R_1 = 0.1$$

or:

$$R_1 = 10 \times R_F$$

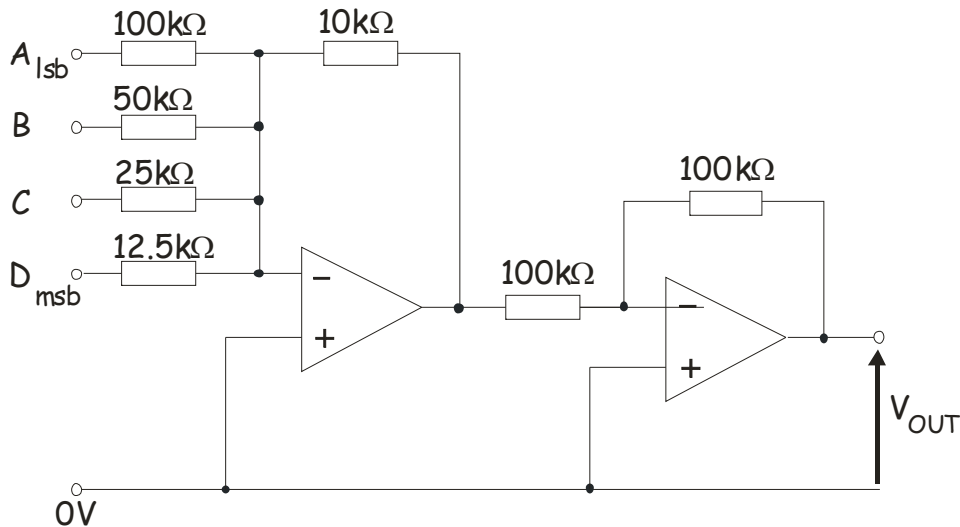
The following values satisfy this requirement:

$$R_F = 10k\Omega$$

$$R_1 = 100k\Omega$$

In order to get the correct weighting for the voltage gains for the four inputs, the input resistors are in the ratio R_1 , $R_1/2$, $R_1/4$ and $R_1/8$.

The final circuit diagram is shown below:



The two resistors used in the second inverting amplifier can have any value, as long as both are equal (to give a voltage gain of -1) and have resistance greater than $1k\Omega$ (to reduce the size of the current flowing in them, and hence the power dissipated.)

Exercise 3 (A solution is given at the end of the topic)

Design a DAC with the following parameters:

- number of input bits = 3;
- output voltage range = 0 to 14V;
- logic 1 = 10V and logic 0 = 0V;
- power supply = +15V / 0V / -15V.

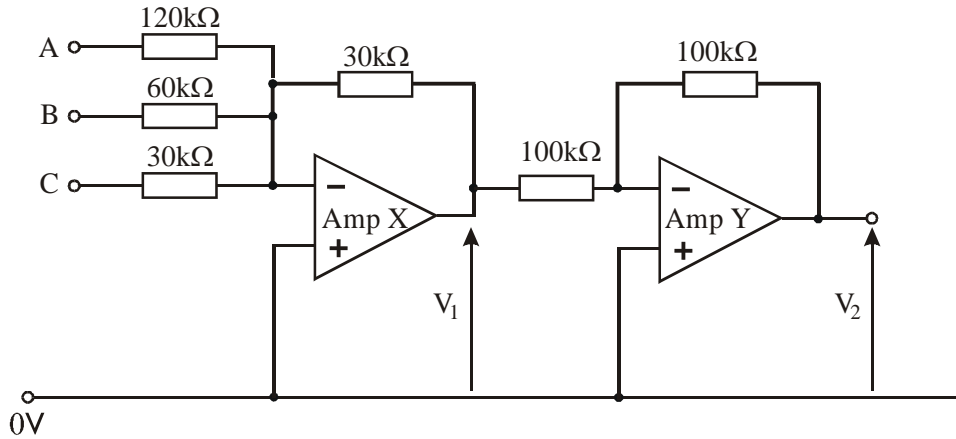
Your design must use the following components:

- 2 op-amps,
- 2 $220k\Omega$ resistors,
- 1 $20k\Omega$ resistor,
- 1 $4k\Omega$ resistor

and two other resistors, for which you must calculate the values

Practice Exam Questions:

1. A microprocessor systems can contain both an analogue-to-digital converter (ADC) and a digital-to-analogue converter (DAC). Here is the circuit diagram for a digital-to-analogue converter (DAC).



The most significant bit of the binary number is applied to input C, and the least significant bit to input A. The outputs of the op-amps saturate at +12V and -12V.

- (i) What is the gain of amplifier Y? [1]

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- (ii) The following voltages are applied to inputs A, B and C.

$$V_A = +5V$$

$$V_B = 0V$$

$$V_C = 0V$$

Calculate:

V_1 [1]

.....

.....

V_2 [1]

.....

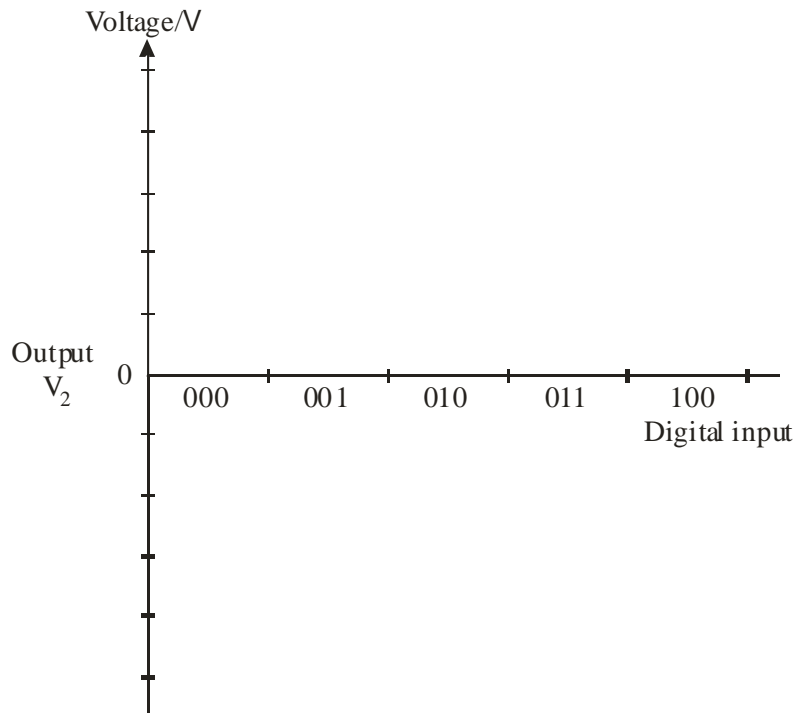
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(iii) The system uses +5V to represent logic 1 and 0V to represent logic 0.

Use the axes provided to draw a graph showing the relationship between V_2 and the digital input signal, for the four values of input given. Indicate the scale you are using for the vertical axis. [2]

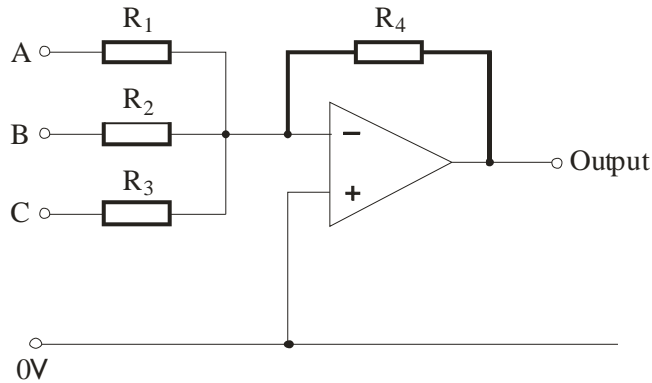


(iv) What is the maximum value of output voltage V_2 that this 3- bit DAC will produce? [1]

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Module ET5
Electronic Systems Applications.

2. (a) The diagram shows the circuit for a 3-bit linear digital-to-analogue converter (DAC), based on a summing amplifier.



- (i) Calculate suitable values for the resistors used in the circuit, so that the DAC has the following characteristics:

Digital input			Output voltage
C	B	A	
0	0	0	0V
0	0	1	- 0.5V

In this system, logic 1 is 12V and logic 0 is 0V.

[3]

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$R_1 = \dots\dots\dots$

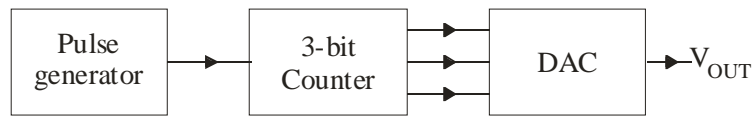
$R_2 = \dots\dots\dots$

$R_3 = \dots\dots\dots$

$R_4 = \dots\dots\dots$

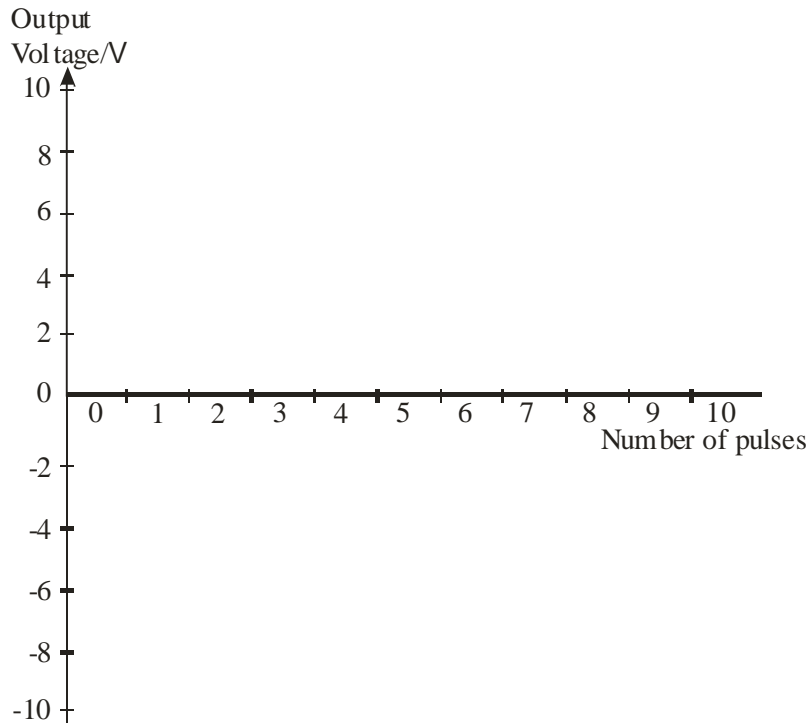
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(ii) The DAC is connected to a counter, as shown in the following diagram.



Initially, the counter is reset. Then ten pulses are sent into the counter. Use the axes provided to sketch the resulting output signal V_{OUT} as this happens.

[3]



Solutions to Exercises:

Exercise 1:

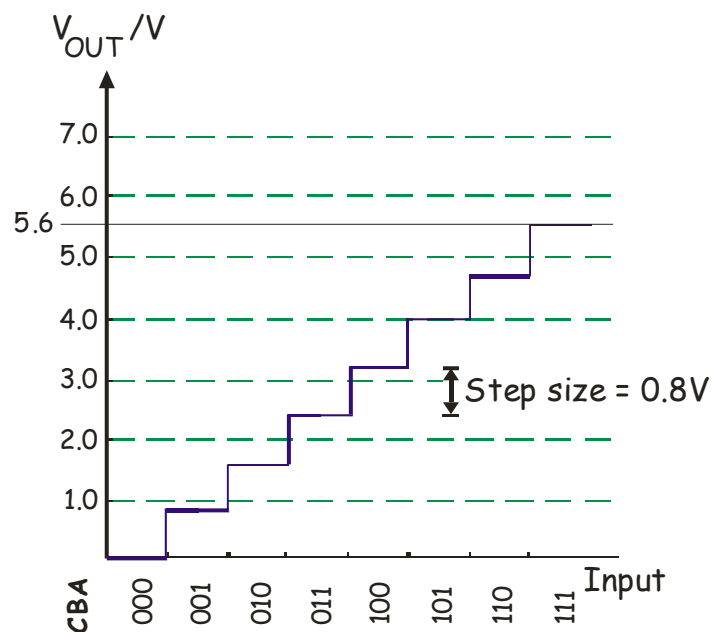
See the results given in the table on page 10.

Exercise 2:

Table of results -

Binary number			V_{OUT} / V
C	B	A	
0	0	0	0
0	0	1	0.8
0	1	0	1.6
0	1	1	2.4
1	0	0	3.2
1	0	1	4.0
1	1	0	4.8
1	1	1	5.6

Graph of results -



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Exercise 3:

