Interfacing Digital to Analogue Circuits

Candidates will be able to:

(a) describe the action of a Schmitt inverter and its use in debouncing signals produced by mechanical switches and analogue sensors

(b) compare the properties of transistors, comparators and Schmitt inverters as interfaces between analogue and digital systems

(c) design interface circuits using npn transistors, MOSFETs and comparators to interface input sensors to outputs

Interfacing Inputs and Outputs

To complete our study of logic systems, we need to look at how to interface inputs and outputs correctly to logic systems. Much of the groundwork for this topic was covered in Component 1 Chapter 4, where we looked at npn transistors, MOSFETS and comparators.

Interfacing to inputs

For a logic gate input to recognise the signal applied to it as logic 1, the voltage level of the signal should be as near as possible to the value of the positive supply rail. Similarly, for the signal to be recognised as logic 0 it should be as near as possible in value to 0 V.

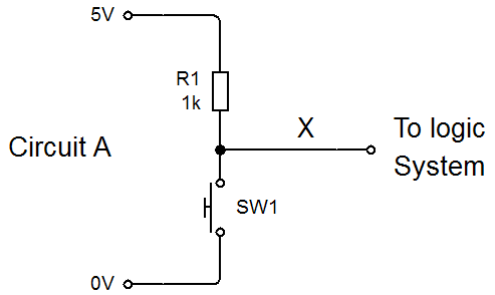
If the input signal changes from logic 0 to logic 1 or from logic 1 to logic 0 it should leap from one to the other as rapidly as possible. This prevents the logic system from behaving in an unpredictable way.

Connecting Mechanical Switches to a Logic System

We have already considered how to connect mechanical switches to the inputs of logic gates using pull-up and pull-down resistors in Component 1 Chapter 6. This is summarised below.

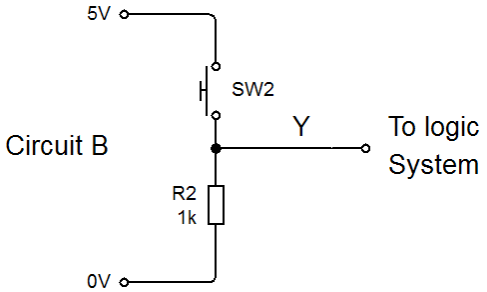
Pull-up resistor

Output signal at point X is normally at logic 1. It changes to logic 0 when the switch is pressed.



Pull-down resistor

Output signal at point Y is normally at logic 0. It changes to logic 1 when the switch is pressed.



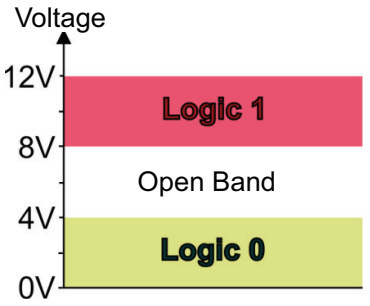
Connecting Sensors to a Logic System

Logic gates are designed to recognise a predetermined band of voltages as representing logic 0 and logic 1. These bands are specific for each family of ICs as seen in the following table:

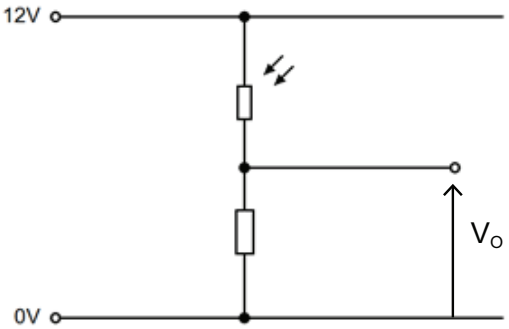
	TTL (74 series)	CMOS (4000 series)
Supply voltage	5 V ± 0.25 V only	3 V to 18 V
Logic 0 range	0 to 0.8 V	Below 30% of supply voltage
Logic 1 range	2.0 to 5.0 V	Above 70% of supply voltage

The intermediate levels or band of voltages below the logic 1 threshold and above the logic 0 threshold result in unpredictable circuit behaviour. This region between the logic 0 and logic 1 bands is sometimes referred to as the **open band**.

The diagram on the right illustrates the three bands for a CMOS logic gate connected to a 12 V power supply.

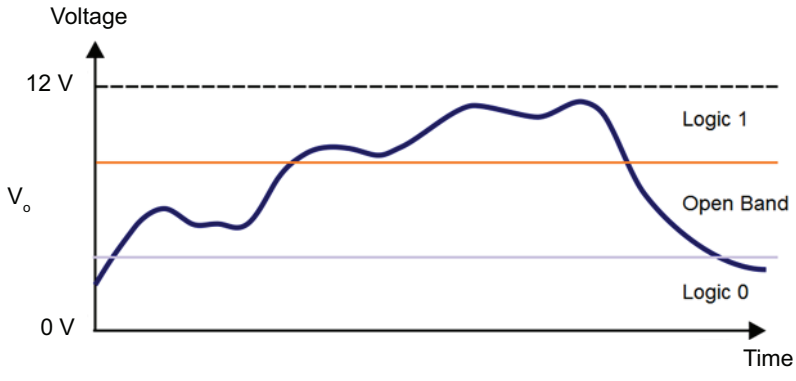


Consider the light-sensing sub-system opposite:



Assume that the light level steadily increases over several hours and eventually decreases again.

Initially this causes the resistance of the light dependent resistor (LDR) to decrease and the output voltage V_O to increase. When the light level eventually decreases, V_O decreases again, as shown in the graph below.



Logic gates require input signals that change rapidly between logic states.The analogue signal shown in the graph could remain in the open band for long periods of time, causing unpredictable behaviour and possible damage of a logic gate with which the sensor is interfaced.

Signal Conditioning

Slow-changing signals from analogue sensing circuits have to be **processed** or **conditioned** before they can be correctly used with logic gates.

Schmitt Inverters

Schmitt inverters are ideal for interfacing input sensors to logic systems. They are particularly useful for improving rise times by converting slowly changing analogue signals into signals that change logic state almost instantly. They have the added advantage of ignoring small changes in the signal produced by the sensing sub-system.

The action of a Schmitt inverter

Ordinary inverters have a single input voltage level which causes the output to change state. This voltage level is referred to as the threshold level. A Schmitt inverter has the same truth table as an ordinary inverter, but it has two switching thresholds rather than one.

The switching threshold for a rising input voltage is higher than that for a falling input voltage. The actual threshold values differ for different types of Schmitt inverter.

A CMOS Schmitt inverter has an upper switching threshold (V_{T+}) of approximately two thirds the supply voltage for a rising input voltage, and a lower switching threshold (V_{T-}) of approximately one third the supply voltage for a falling input voltage. On a 5 V supply this would give switching thresholds of approximately 3.3 V and 1.6 V.

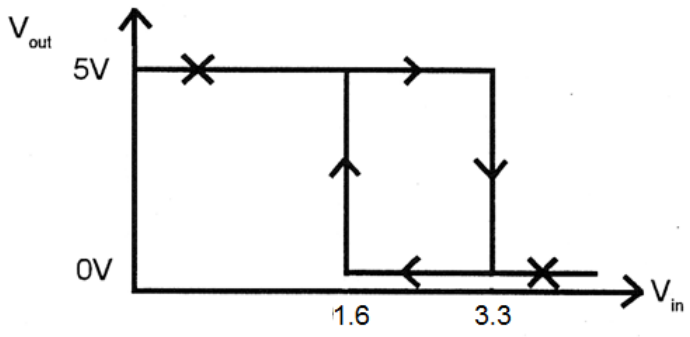
On a 5 V supply, a TTL 7414 Schmitt inverter has an upper switching threshold of approximately 1 .7 V and a lower switching threshold of 0.9 V.

This means that:

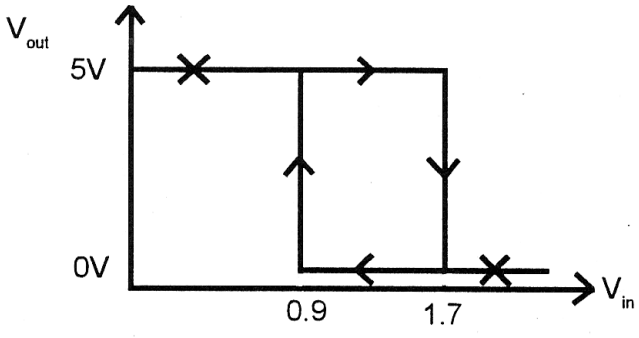
- when the input voltage is at 0 V the output is at logic 1;
- as the input voltage increases, the output remains at logic 1 until the input voltage reaches the upper threshold;
- then, the output abruptly changes to logic 0 and remains there until the input voltage drops below the lower threshold;
- then the output will abruptly change back to logic 1.

This action of a Schmitt inverter when connected to a 5 V supply is summarised in the graphs below.

CMOS



TTL



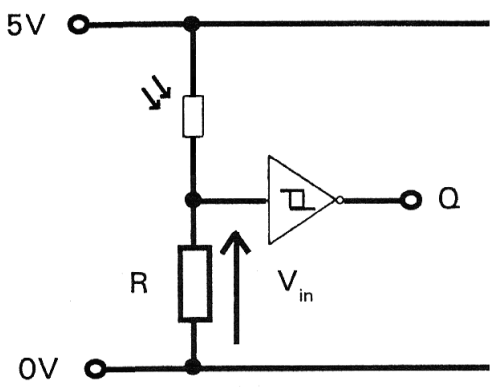
The Schmitt inverter has a dual purpose:

(i) It converts a slowly changing signal to an abruptly changing signal once the **input threshold voltage** has been reached.

(ii) The gap or 'deadband' between the threshold for a rising input voltage and a falling input voltage prevents minor changes in the sensor signal from rapidly switching the output logic level repeatedly between logic 0 and 1.

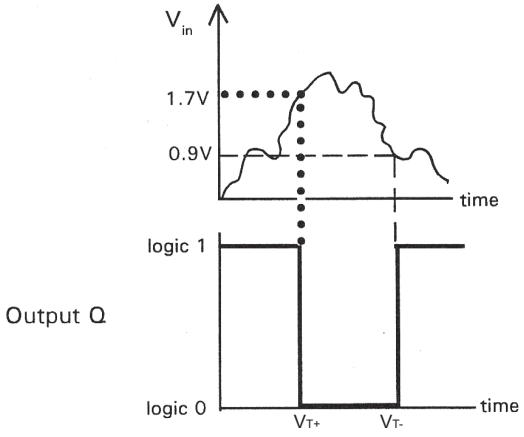
Improving the rise time of a sensing sub-system

The signal from a light-sensing unit is applied to a Schmitt inverter.



- In darkness the resistance of the LDR is very high, the input voltage (V_{in}) is nearly 0 V, and the output is at logic 1.
- V_{in} increases gradually as the light level increases.
- The output, Q, remains at logic 1 until V_{in} reaches the upper switching threshold (V_{T+}).
- Then, the output changes almost instantly to logic 0 and remains there until V_{in} falls to (V_{T-}).
- Then, the output changes almost instantly to logic 1.

Typical behaviour is shown in the graph opposite.



Notice the rapid transitions between output logic levels, as the input signal reaches the threshold voltages.

Minor fluctuations in input voltage are ignored.

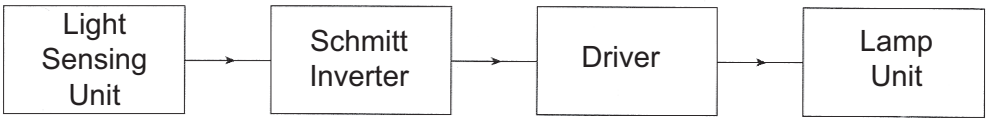
The Schmitt inverter has conditioned the input signal to make it suitable for a logic system.

A similar result would occur if the light-sensing sub-system were to be replaced with a temperature-sensing sub-system.

A **comparator** could be used to improve the rise time of a sensing sub-system but, as there is no deadband, minor changes in the signal from the sensor near the switching threshold could cause the comparator output to switch rapidly and repeatedly between logic 0 and 1.

Example:

The block diagram shows the design of a security light, which turns on automatically when it gets dark.



a) What is the purpose of the Schmitt inverter in this system?

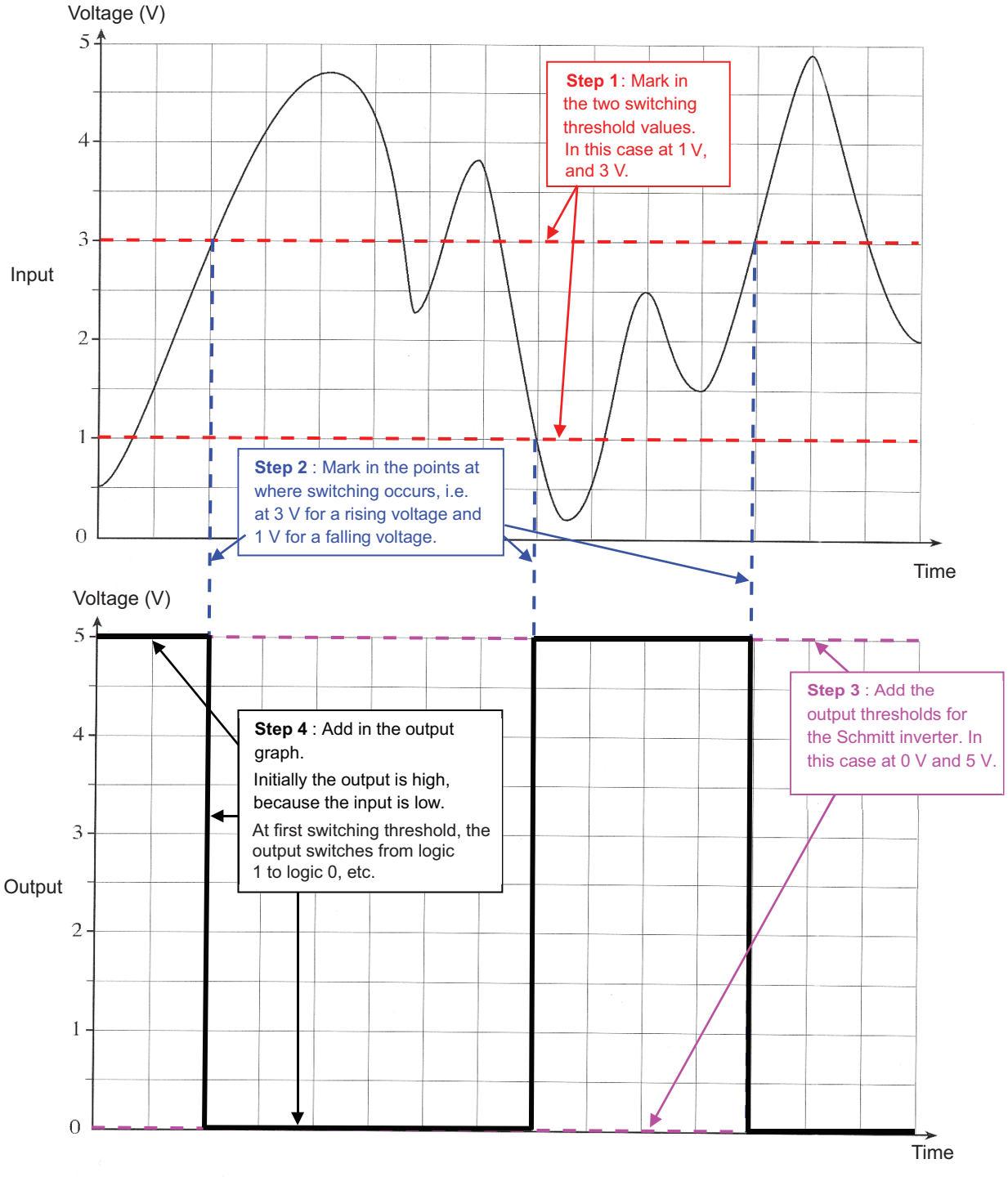
Answer: The Schmitt inverter acts as an interface between a slowly changing light level and produces a fast changing output when the threshold light level is reached.

b) Here is part of a data sheet for a Schmitt inverter:

When connected to 5 V supply:

- Logic 0 = 0 V
- Logic 1 = 5 V
- The output changes from logic 1 to logic 0 when a **rising** input voltage reaches 3 V
- The output changes from logic 0 to logic 1 when a **falling** input voltage reaches 1 V

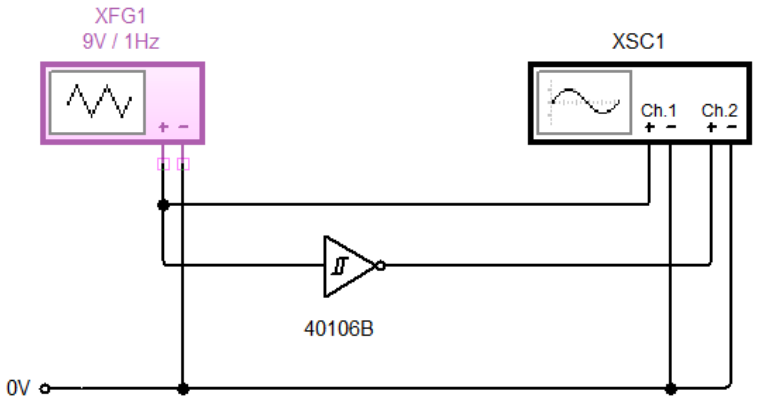
The input signal for the Schmitt inverter is shown below.
Use the axes provided to draw the resulting output signal produced by the Schmitt inverter.

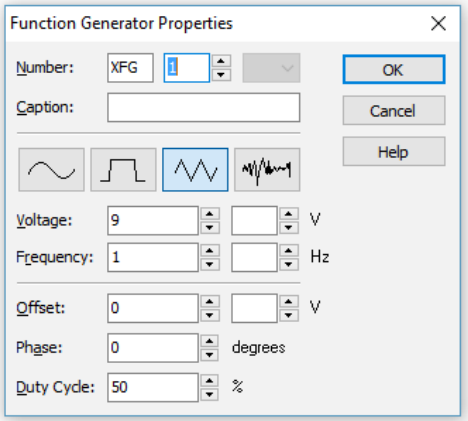


Investigation 3.1

Set up the following circuit with the function generator output adjusted to the settings shown to produce a triangular waveform.

If you are setting this circuit up on Circuit Wizard ensure that the voltage setting for the CMOS 40106 IC is set to 9 V. Go to ***Project*** >> ***Simulation*** >> ***Power supply*** and set the voltage to 9 V.



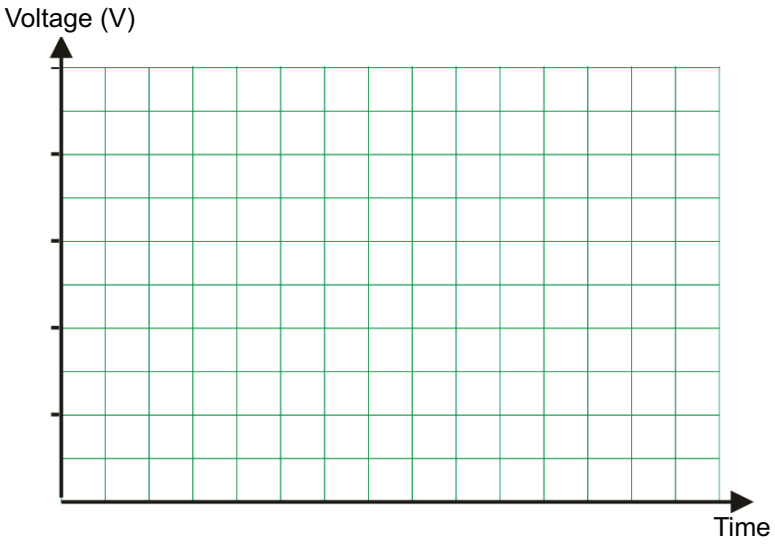


Set the oscilloscope time base to 100 ms.

a) Study the oscilloscope display and determine the switching thresholds for the Schmitt inverter.

.....

b) Sketch the input and output waveforms obtained on the graph grid below. Label both axes with appropriate scales and use a different colour to represent the input and output waveforms.



Exercise 3.1

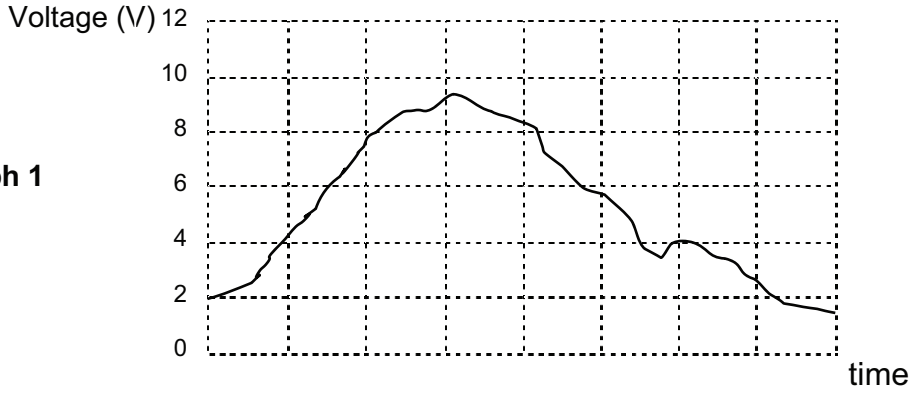
1. Here is part of a data sheet for the Schmitt inverter:

When connected to a 12 V supply:
- Logic 0 = 0 V
- Logic 1 = 12 V
- The output changes from logic 1 to logic 0 when a **rising** input voltage reaches 5 V
- The output changes from logic 0 to logic 1 when a **falling** input voltage reaches 3 V

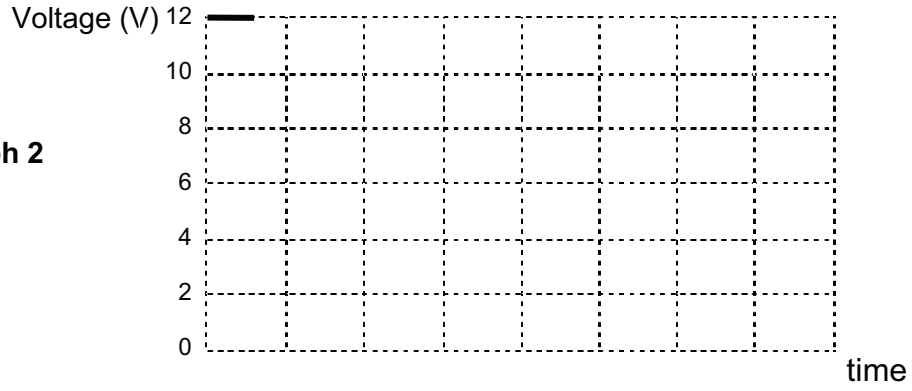
The output signal produced by a temperature-sensing unit is shown in **Graph 1**.

Complete **Graph 2** to show the signal obtained at the output of the Schmitt inverter.

Graph 1



Graph 2

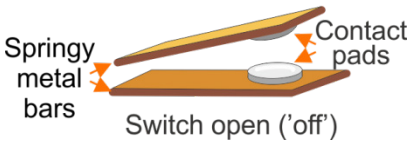


Interfacing Mechanical Switches to Count and Display Systems

Switch bounce

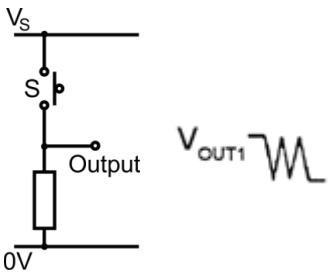
The contact blades of both mechanical and reed switches tend to ‘bounce’ when the switch is closed.

A switch is simply two metal bars, separated by air when switched ‘off’ and pressed into contact when ‘on’.



When the springy metal bars flick into contact, they bounce off again and can do so a number of times.

When the switch is closed, the bounces make the output change rapidly between logic 0 and logic 1 several times before settling down. This effect is known as switch bounce.

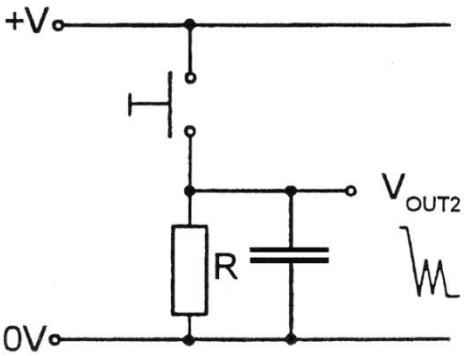


The graph below shows the results of switch bounce on the output of a switch unit:

Switch bounce has little effect in a system consisting only of logic gates. If the system contains a counter, then switch bounce is highly undesirable. The counter will jump by several numbers each time the switch is pressed, as it counts each of the bounces. This bouncing is usually finished within a few milliseconds.

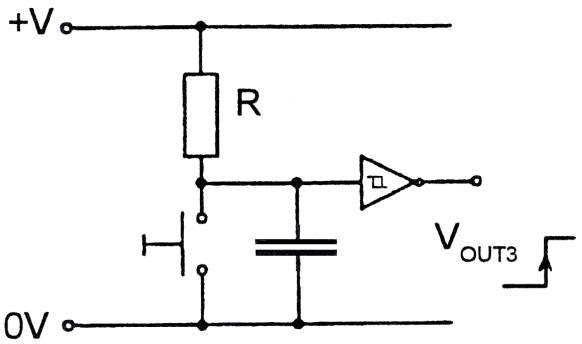
Switch debouncing

A capacitor, connected across the switch, will suppress but not completely eliminate the effect of the contact blades bouncing.



Adding a Schmitt inverter will eliminate any effect of switch bounce on the output. Notice that we have swapped over the positions of the switch and resistor to take account of the inverting action of the Schmitt inverter.

The small fluctuations in $\mathbf{V_{OUT2}}$ are ignored by the Schmitt inverter. The output V_{OUT3} is said to be 'debounced'.

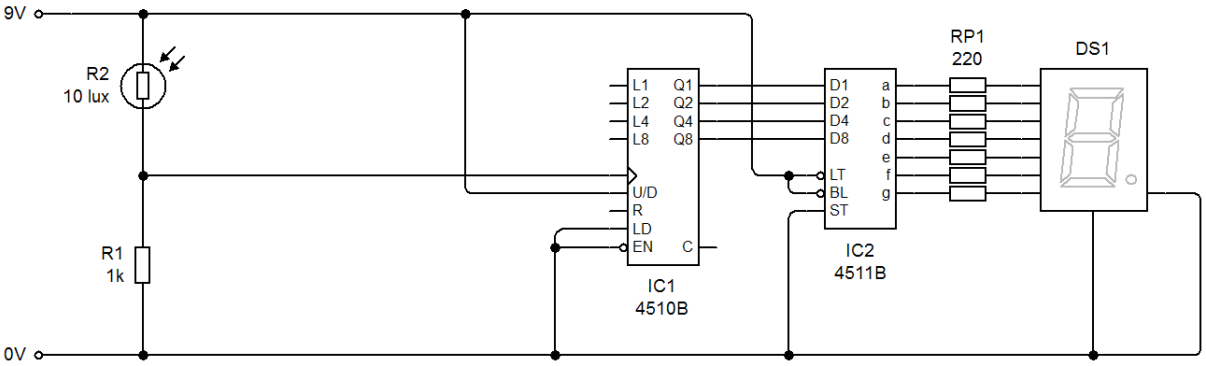


The value of capacitor used depends on how fast you want to count. A value in the range 1–10 μF works well for most applications.

Investigation 3.2

1. Connecting a light sensor to a counting system

a) Set up the circuit below, which is used to count the number of people boarding a fairground ride. A light beam is broken as someone walks through it.

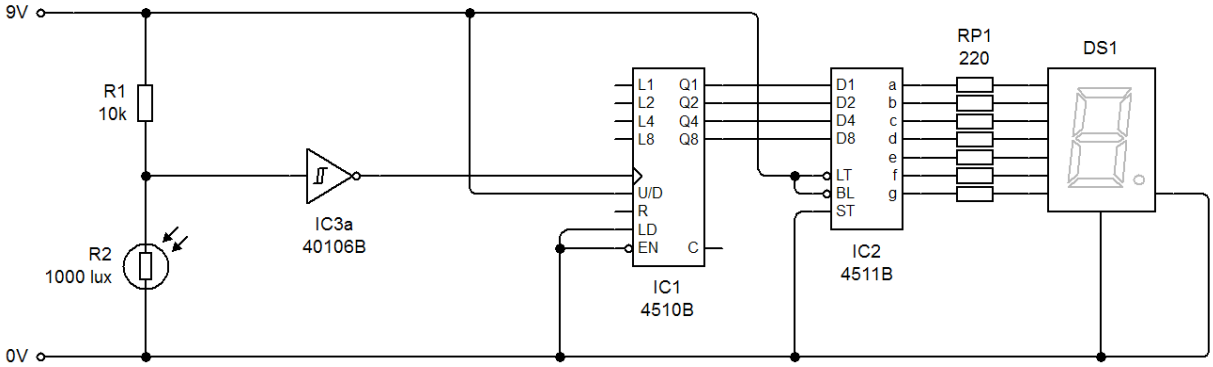


b) Comment on how well the system works as the light level falling on the LDR changes. Try changing the light level both slowly and quickly.

.....

.....

c) You should have observed that the system only counts when the light level is changed very quickly. Modify the circuit as shown below:



d) Is the performance of the system better? Give a reason for any change.

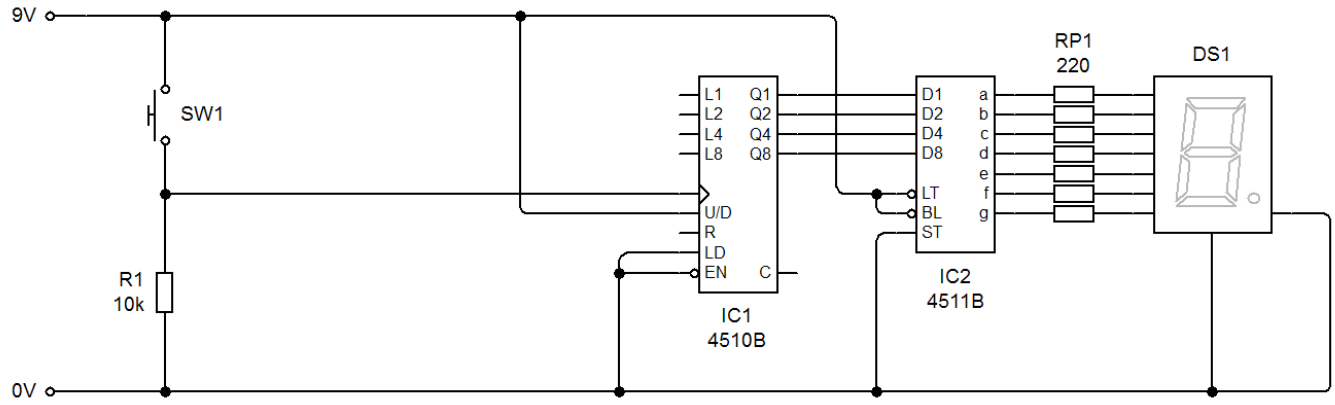
.....

.....

2. Switch bounce

If you are setting this circuit up on Circuit Wizard go to ***Project*** >> ***Simulation*** and click on >> ***Bounce.***

a) Set up the following counting system.



b) Press switch SW1 several times. You will probably get an unexpected result. Can you give a reason why?

.....

.....

c) Add a debounce circuit to the input using a 10 µF capacitor and a 40106 Schmitt inverter. (You will also have to make one other change to the circuit.) Comment on the accuracy of the count.

.....

d) Does changing the capacitor value to 1 µF have any affect?

.....

Interfacing Logic Systems to Outputs

Logic gates can only provide an output current of a few milliamps when the output is at logic 1. If the output current is increased beyond this, the output voltage drops. The larger the value of output current the smaller is the output voltage. (This effect is similar to the loading of a voltage divider circuit that we considered in Component 1 Chapter 3.)

Directly connected outputs

Output devices that require a current of about 10 mA or less can be connected directly to a TTL output. This value is reduced to about 5 mA for a CMOS output. This limits directly connected outputs to LEDs and low power buzzers.

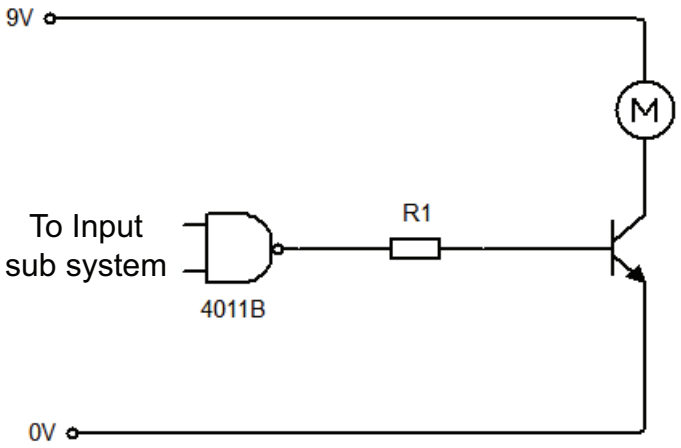
Connecting logic gates to larger loads

Output devices that require a current of more than 10 mA can be interfaced to a logic system using a transistor or a MOSFET.

Example 1:

- The NAND gate can provide a current of 5 mA when its output voltage is 7 V.
- The motor has a rated current of 240 mA

The transistor just saturated when its input voltage is 7 V.



a) Calculate the value of R1 which will limit the base current to 5 mA .

Solution:

Voltage drop across R1:

$$R1 = 7 - 0.7 = 6.3\ V$$

Value of R1:

$$R1 = \frac{V}{I} = \frac{6.3\ V}{5\ mA} = 1.26\ K\Omega$$

b) Calculate the value of h_{FE} of the transistor to allow the motor to work at its rated current.

$$h_{FE} = \frac{I_C}{I_B} = \frac{240}{5} = 48$$

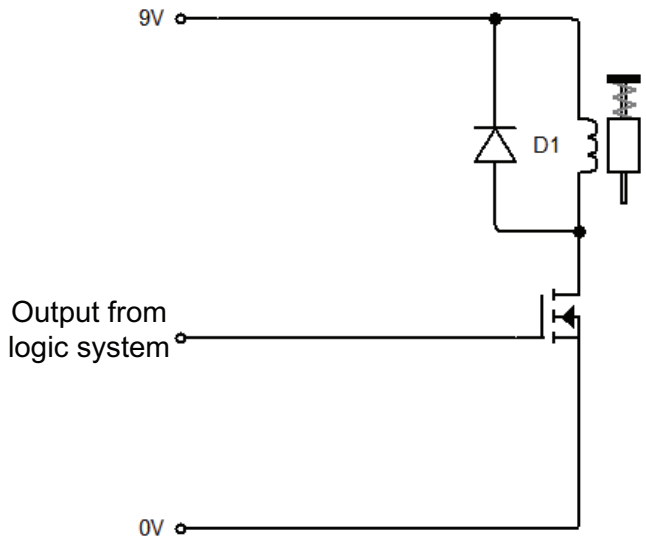
A MOSFET is very useful for interfacing CMOS logic gates to high power DC, since it is voltage operated and requires almost zero gate current to switch it on.

Example 2:

A logic system is used to control a solenoid. The solenoid is rated at 9 V, 5 A and the MOSFET has a value of $g_M = 1.25$ S.

Calculate the minimum output voltage of the logic system to allow the solenoid to work at its rated current.

$$I_D = g_M(V_{GS} - 3)$$
$$5 = 1.25(V_{GS} - 3)$$
$$\frac{5}{1.25} = V_{GS} - 3$$
$$4 = V_{GS} - 3$$
$$V_{GS} = 4 + 3 = 7 \text{ V}$$



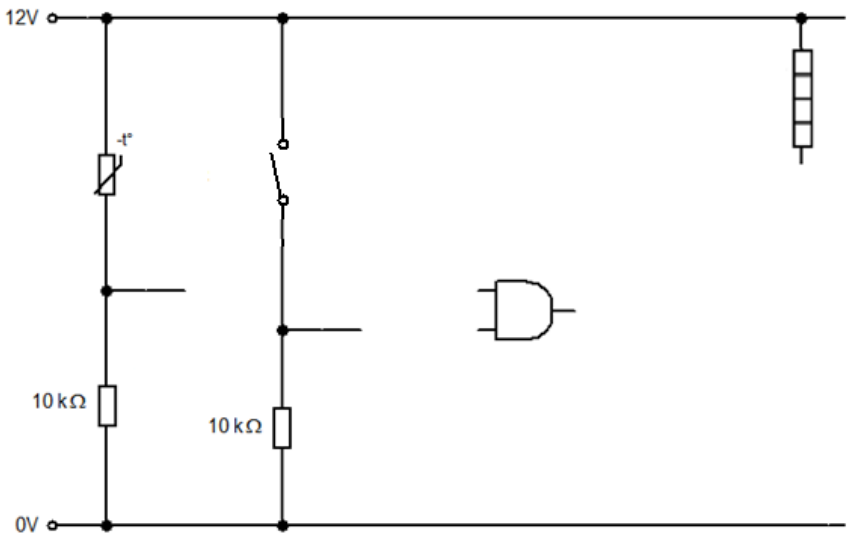
Note:

- If a transistor interface were to be used for this application it would require a collector current rating of 5 A and current gain (h_{FE}) equal to 5 A / 10 mA = 500.
- It is virtually impossible to get a transistor with both of these parameters. The MOSFET overcomes this problem.

Exercise 3.2

1. A heater is required for a small greenhouse. The heater which is rated at 12 V, 6 A should only come on when a master switch is closed and the temperature drops below a certain value.

a) Complete the circuit diagram for the system by adding additional components and connections.

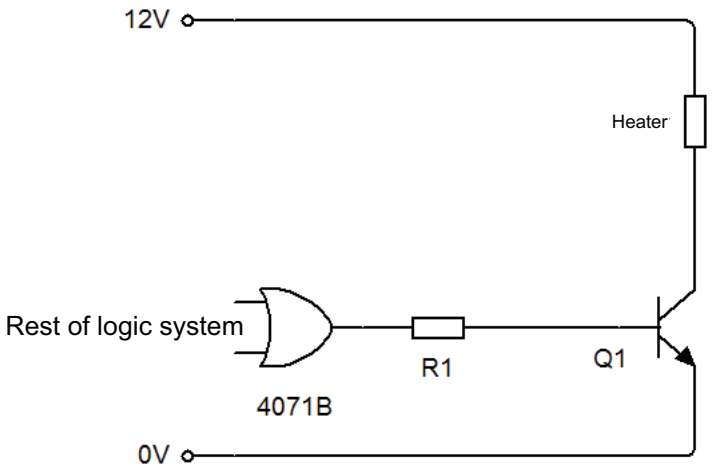


b) Give a reason for choosing the additional components.

.....

.....

2. The final output of a logic system comes from an OR gate and uses a transistor to drive a high power heater as shown in the circuit diagram below:



- The OR gate can provide a maximum output current of 4.5 mA when its output voltage is 11 V.
- The heater has a rated current of 3.6 A.

The transistor just saturated when its input voltage is 11 V.

a) Calculate the value of R1 which will limit the base current to 4.5 mA.

.....

.....

.....

.....

.....

.....

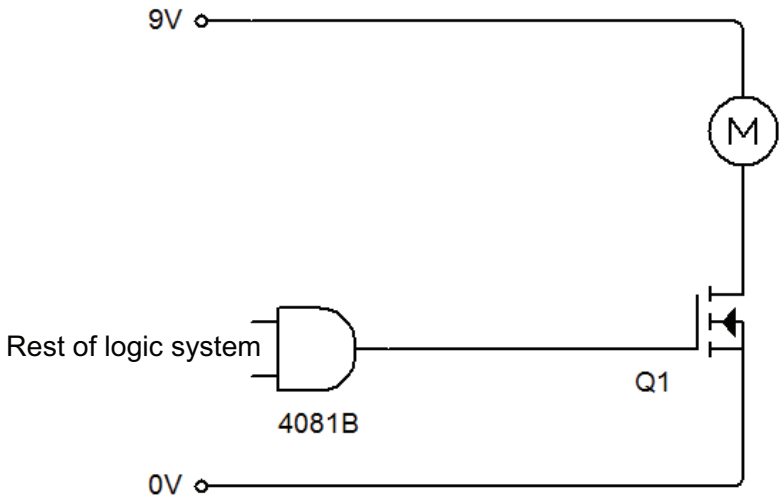
b) Calculate the value of h_{FE} to allow the motor to work at its rated current.

.....

.....

.....

3. A logic system is used to control a motor.



The motor is rated at 9 V, 8 A and the MOSFET has a value of g_M = 1.6 S.

a) Calculate the minimum output voltage of the logic system to allow the solenoid to work at its rated current.

.....

.....

.....

.....

.....

.....

.....

.....

.....

.....

b) Add a component to the circuit to protect the transistor from high reverse voltages.