Chapter 2: Timing Circuits

1. RC Networks

Learning Objectives:

At the end of this topic you should be able to:

- explain how capacitors can be used to form the basis of timing circuits;
- calculate the value of the time constant for an **RC** circuit using **T** = **R** × **C**;
- sketch capacitor charge and discharge curves for both voltage and current;
- select and use the following formulae:
  - $V_C = V_0 \times \left(1 - e^{-\frac{t}{RC}}\right)$ or a charging capacitor;
  - $V_C = V_0 \times e^{-\frac{t}{RC}}$ for a discharging capacitor;
- recall that:
  - V_C = 0.5 V_0 after 0.69 **RC**;
  - $V_C \approx V_0$ after 5 **RC** for charging capacitors;
  - $V_C \approx$ 0V after 5 **RC** for discharging capacitors.

Introduction

Timing circuits are used in a wide variety of applications – from short time delays of a few nanoseconds used in digital circuitry and computers to long periods of hours used to control household appliances and industrial processes. Electronic timing circuits provide this function reliably and accurately, without any user input or monitoring once the time has been set.

RC networks are the basic circuit elements controlling timing circuits. The capacitor charges or discharges at a rate determined by the size of the capacitor and the size of the resistor.

These two factors are combined in the 'time constant', **T**.

In other words, time constant **T** = **R** × **C**. It can be shown that the units of time constant are seconds when **R** is in ohms and **C** is in farads, or **R** is in megohms and **C** is in microfarads.

Example:

Calculate the time constant of a circuit containing a 10 kΩ resistor and a 470 μF capacitor.

Time constant = **R** × **C**.
= 10 kΩ × 470 μF
= $10 \times 10^3 \times 470 \times 10^{-6}$
= 4.7 s

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Exercise 2.1

1. Calculate the time constant for the following resistor / capacitor combinations:

a) **R** = 2.2 MΩ, **C** = 330 µF.
.....

b) **R** = 4.7 kΩ, **C** = 1000 µF.
.....

c) **R** = 470 kΩ, **C** = 8.2 nF.
.....

d) **R** = 1.8 MΩ, **C** = 470 pF
.....

2. A timing circuit requires an **RC** network with a time constant of 33 seconds.
What value of resistance would provide this time constant, used with a 22 µF capacitor?
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3. What value of capacitance provides a time constant of 30 ms when used with a 10 kΩ resistor?
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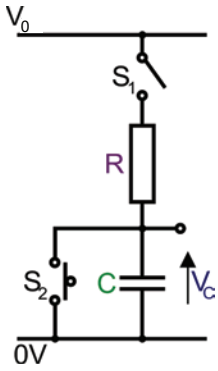
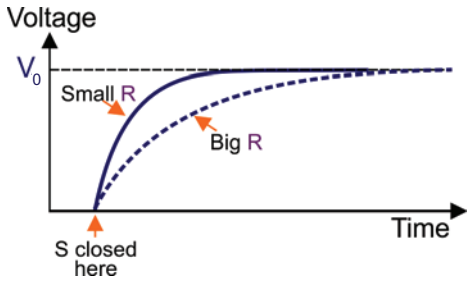
Charging a Capacitor

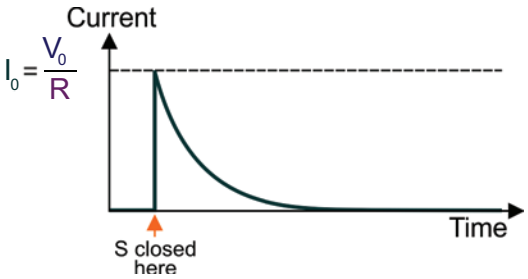


The circuit opposite can be used to investigate the charging process.
Momentarily, press switch S_2 so that the capacitor is initially uncharged (0V).
When switch S_1 is closed, the full supply voltage, V_0, appears across the resistor **R** and so an initial current I_0 flows through it.
This current, I_0, can be calculated from the Ohm's law formula since the voltage across the resistor is the full supply voltage:

$$I_0 = \frac{V_0}{R}$$

This current charges up the capacitor and V_C rises, the voltage across the resistor (= $V_0 - V_C$) and reduces the current flowing through it.
The capacitor continues to charge but not as quickly.
Eventually, V_C reaches the supply voltage, V_0. The voltage drop across the resistor and the current through it fall to zero. The capacitor is fully charged.
Without switch S_2, the capacitor would, in theory, remain charged to V_0 and the investigation could not be repeated. Pressing S_2 discharges the capacitor, allowing the investigation to be repeated.
The charging behaviour is shown in the graphs that follow, though a curve obtained experimentally may not reproduce them exactly, as the approach outlined above assumes that the capacitor has ideal characteristics and, in particular, that there is no leakage current.
The left-hand graph below shows the voltage behaviour for a big resistor (and big time constant) and for a small one (and small time constant).
The right-hand graph below shows the equivalent behaviour for current with the small resistor.





The voltage curve is called exponential growth, as it involves the exponential constant 'e'. It can be shown that the voltage across the capacitor, V_C, obeys the equation:

$$V_C = V_0 \times \left(1 - e^{-\frac{t}{RC}}\right)$$ where t is the time elapsed since the switch was closed.

This relationship leads to the following rules of thumb:

- $V_C = 0.5\ V_0$ after $0.69\ RC$;
  (demonstrated in a few pages time!)
- $V_C \approx V_0$ after $5\ RC$ for charging capacitors.
  (Using: $V_C = V_0\ (1 - e^{-5RC/RC})$,
  $V_C = V_0\ (1 - e^{-5})$
  $= V_0\ (0.993)$
  i.e V_C = 99.3% of V_0 after $5\ RC$)

(Mathematically, it takes infinite time to charge the capacitor fully!)
The current graph is called exponential decay. Similar results apply to current:

- $I = 0.5\ I_0$ after $0.69\ RC$;
- $I \approx 0$ after $5\ RC$.

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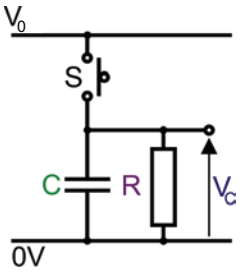
Capacitor Discharge



The circuit opposite can be used to investigate the discharge behaviour of a capacitor.

When switch **S** is closed, the capacitor is connected directly to the power supply. As there is virtually no resistance in the current path, the capacitor charges up almost instantly to the supply voltage.

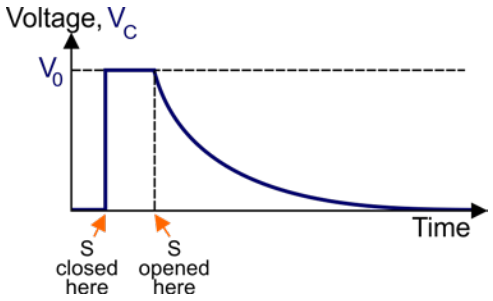
When **S** is opened, the capacitor is charged up to $\mathbf{V_0}$, the full supply voltage. Resistor **R**, connected in parallel, experiences the same voltage. As a result, a current I flows through the resistor.

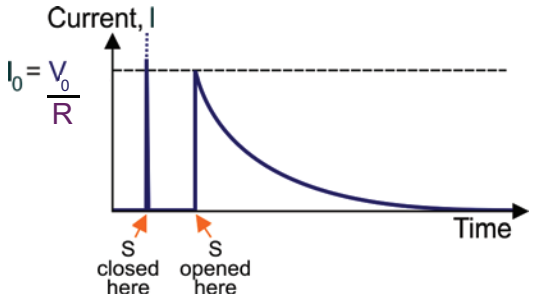
This current comes not from the power supply but from the charged capacitor. Hence, the capacitor begins to discharge – the voltage across it falls.

Likewise, the voltage across the resistor and the current through it fall. The discharge of the capacitor slows down. Eventually, the capacitor is fully discharged – the voltage across it is zero.

This arrangement does not require a second switch, as the capacitor finishes uncharged, allowing the investigation to be repeated directly.

The discharge behaviour is shown in the graphs that follow.





This time, the voltage curve, showing capacitor discharge, is called exponential decay.

It can be shown that this voltage across the capacitor, $\mathbf{V_C}$, obeys the equation:

$$V_C = V_0 \times e^{-\frac{t}{RC}}$$

where:

- t is the time elapsed since the switch was opened;
- $\mathbf{V_0}$ is the initial voltage across the capacitor (not necessarily the supply voltage).

This results in the following 'rules of thumb':

- $\mathbf{V_C}$ = 0.5 $\mathbf{V_0}$ after 0.69 **RC**;
- $\mathbf{V_C} \approx$ 0 V after 5 **RC**.

The current graph also shows exponential decay. Similar results are:

- **I** = 0.5 $\mathbf{I_0}$ after 0.69 **RC**;
- **I** ≈ 0 after 5 **RC**.

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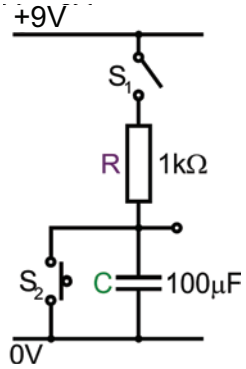
Example 1:



Initially, switch S_2 is pressed for a moment to discharge the capacitor.
Switch S_1 is closed at time t = 0.
Find the voltage across the capacitor at time:

- t = 0.05 s;
- t = 0.25 s.

The circuit is a charging circuit, and so the formula required is:

$$V_C = V_0 \times \left(1 - e^{-\frac{t}{RC}}\right)$$

First of all, calculate the time constant:

Time constant T = **R** × **C**.
= 1 kΩ × 100 μF
= $1 \times 10^3 \times 100 \times 10^{-6}$
= 0.1 s

Next, the voltages across the capacitor:

i) at 0.05 s

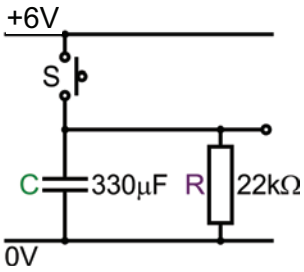
$$V_C = V_0 \times \left(1 - e^{-\frac{t}{RC}}\right)$$
$$= 9 \times \left(1 - e^{-\frac{0.05}{0.1}}\right)$$
$$= 9 \times (1 - 0.6065)$$
$$= 3.54 \text{ V}$$

ii) at 0.25 s

$$V_C = V_0 \times \left(1 - e^{-\frac{t}{RC}}\right)$$
$$= 9 \times \left(1 - e^{-\frac{0.25}{0.1}}\right)$$
$$= 9 \times (1 - 0.0821)$$
$$= 8.26 \text{ V}$$

At 0.05 s, the voltage across the capacitor is 3.54 V.
At 0.25 s, the voltage across the capacitor is 8.26 V.

Example 2:



In the circuit shown opposite, the switch is closed for a moment.
It is then opened at time t = 0.

Calculate the voltage across the capacitor at times t = 3 s and t = 6 s.

The capacitor discharges when the switch is opened, and the formula required is: $V_C = V_0 \times e^{-\frac{t}{RC}}$

Firstly, the time constant:

Time constant T = **R** × **C**.
= $22 \times 10^3 \times 330 \times 10^{-6}$
= 7.26 s

Next, the voltages across the capacitor:

i) at 3 s

$$V_C = V_0 \times e^{-\frac{t}{RC}}$$
$$= 6 \times e^{-\frac{3}{7.26}}$$
$$= 6 \times 0.6615$$
$$= 3.97 \text{ V}$$

ii) at 6 s

$$V_C = V_0 \times e^{-\frac{t}{RC}}$$
$$= 6 \times e^{-\frac{6}{7.26}}$$
$$= 6 \times 0.4376$$
$$= 2.63 \text{ V}$$

At 3 s, the voltage across the capacitor is 2.63 V. At 6 s, the voltage across the capacitor is 3.97 V.

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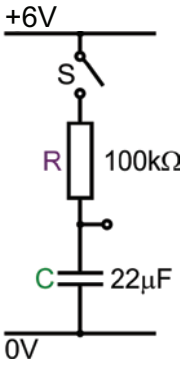
Exercise 2.2

1. The capacitor in the circuit opposite is initially uncharged.
The switch is closed at time t = 0.
Find the voltage across the capacitor at time:

- t = 0.5 s;
- t = 8 s.



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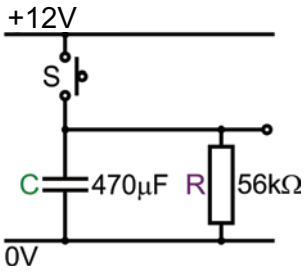
2. In the circuit opposite, the switch is closed for a moment and then opened at time t = 0.
Calculate the voltage across the capacitor at times t = 15 s and t = 40 s.



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Calculating Charge and Discharge Times

The emphasis now changes from calculating the voltage across the capacitor after a specific time to calculating the time taken for a specific change in voltage to occur.

Rearranging the formulae given earlier gives:

- for a charging capacitor: $t = -R.C.\ln\left(1 - \frac{V_C}{V_0}\right)$
- for a discharging capacitor: $t = -R.C.\ln\left(\frac{V_C}{V_0}\right)$

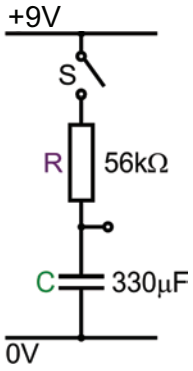
Both formulae use the 'natural logarithm' of an expression.

This is not the same as 'log' on your calculator. Be careful to use the 'ln' function.

In both of these formulae, the '×' (multiplication) sign has been replaced with a '.' which also means 'multiplied by'. Sometimes there is no multiplication sign at all.

For example: $t = -RC\ln\left(1 - \frac{V_C}{V_0}\right)$

Example 1:



The capacitor in the circuit opposite is initially uncharged.
Switch S is closed at time t = 0.

Calculate the time taken for the capacitor to charge to 6 V.

First, calculate the time constant as usual:

Time constant = **R** × **C**.

$= 56\ k\Omega \times 330\ \mu F$

$= 56 \times 10^3 \times 330 \times 10^{-6}$

$= 18.48\ s$

Next, calculate the time taken:
Using the formula: $t = -RC\ln\left(1 - \frac{V_C}{V_0}\right)$

$t = -18.48 \times \ln\left(1 - \frac{6}{9}\right)$

$t = -18.48 \times \ln(0.3333)$

$t = -18.48 \times -1.10$

$t = 20.30\ s$

The time taken to charge to 6 V is 20.30 s.

The voltage reaches 6 V in 20.30 seconds after the switch is closed.

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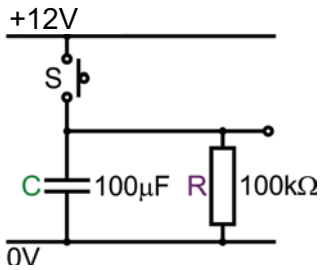
Example 2:



In the circuit opposite, the switch is closed for a few seconds and then reopened at time t = 0 s.

How long does it then take for the voltage across the capacitor to fall to ½V_0 (6 V in this case)?

First, the time constant:

Time constant = **R** × **C**.
= 100 kΩ × 100 µF
= 100 × 10^3 × 100 × 10^{-6}
= 10 s

Then the time calculation:
Using:

$$t = -R.C.\ln\left(\frac{V_C}{V_0}\right)$$

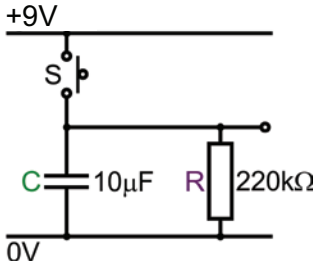
$$t = -10 \times \ln\left(\frac{6}{12}\right)$$

$$t = -10 \times \ln(-0.6931)$$

$$t = 6.93 \text{ s}$$

It takes 6.93 s to decay to ½ V_0

Example 3:



This calculation is independent of supply voltage. The 'ln' expression, 'ln $\left(\frac{V_C}{V_0}\right)$ always reduces to 'ln(0.5)' (= –0.6931) when looking for the time when V_C = ½V_0.
The time taken to charge to half of the supply voltage (from 0 V) or discharge to it (from V_0) is known as the half-life, τ, of the **RC** network.
In the circuit shown, the switch is closed to charge up the capacitor. At time t = 0 s, the switch is then opened.
How long does it take for the voltage across the capacitor to fall from 4.5 V to 2 V?
First, the time constant:

Time constant = **R** × **C**.
= 220 kΩ × 10 µF
= 220 × 10^3 × 10 × 10^{-6}
= 2.2 s

The time calculation is in two parts:

1. Time taken to discharge from 9 V to 2 V:
   Using the equation: $t = -R.C.\ln\left(\frac{V_C}{V_0}\right)$

$$t = -2.2 \times \ln\left(\frac{2}{9}\right)$$

$$t = 3.31 \text{ s}$$

2. Time taken to discharge from 9 V to 4.5 V:
   Recognising that 4.5 V is half of the V_0, we can use the result given earlier:
   t = 0.69.**R**.**C**
   = 1.52 s
   For the voltage to fall from 4.5 V to 2 V takes 3.31 – 1.52 = 1.79 s.

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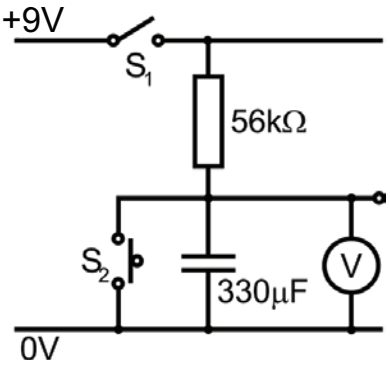
Investigation 2.1

Note: If using 'Circuit Wizard', ensure that you are taking readings in real time by going to: *Project / Simulation / Timing Control* and changing the *Time Base* to 1 s.

A. Set up the circuit show on the right**.**



Each time you start this investigation, ensure that the capacitor is discharged by momentarily closing switch $\mathbf{S_2}$.

a) Close switch $\mathbf{S_1}$ and use a stopwatch to measure how long it takes for the voltage across the capacitor to rise to 6 V.

Time = ... s.

b) Compare your answer with that given in **Example 1**. Suggest reasons for any discrepancies.

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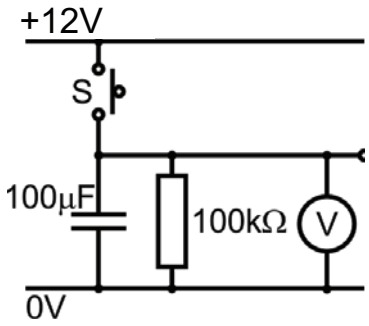
c) Repeat the procedure, and time how long it takes for the capacitor to charge up to 8.5 V.

Time = ... s.

B. Set up the circuit show on the right**.**



a) Momentarily close switch **S** and use a stopwatch to measure how long it takes for the voltage across the capacitor to fall to 6 V.

Time = ... s.

b) Compare your answer with that given in **Example 2**. Suggest reasons for any discrepancies.

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c) Momentarily close **S** again and record the voltmeter reading after 20 s.

Voltage = ... V.

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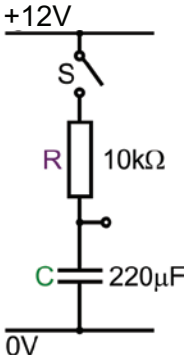
Exercise 2.3

1. In the circuit shown, the capacitor is initially uncharged.
The switch is closed at time t = 0.



a) How long will it take for the voltage across the capacitor to rise to 9 V?

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b) Estimate the time taken for the capacitor to charge fully.

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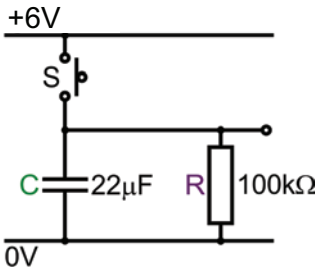
2. Switch S is closed and charges the capacitor almost instantly.



a) Calculate how long it takes for the output voltage to fall to 3 V, once the switch is released

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b) How long does it take for the output voltage to fall from 3 V to 2 V, after the switch is released?

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2. Monostable Circuits

Learning Objectives:

At the end of this topic you should be able to:

- recall that a monostable circuit has one stable state and one unstable state;
- describe how an inverter can be used with a **RC** network as a simple time delay circuit;

Introduction

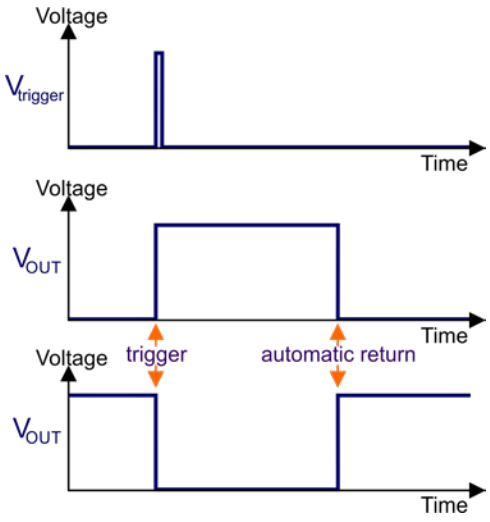
Monostable circuits are useful for creating delay sub-systems of configurable length.

For example, these can be used:

- to keep an outside lamp on for twenty seconds when triggered by a movement sensor;
- to set the heating time for an automatic egg boiler.

Ideal Monostable Behaviour

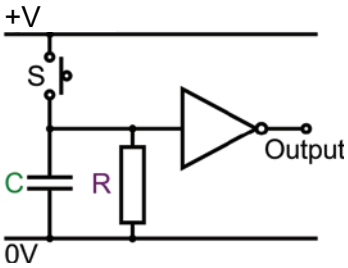
A monostable circuit has one stable state, either logic **0** or logic **1**.
It remains in that state until triggered into the opposite logic state by an external signal.
After a predetermined time, the output returns to the original stable state.
This behaviour is shown in the voltage / time graphs for initially low or high situations.



Buffering the RC network

The basic building block of any monostable timer is the **RC** network.
However, the treatment in section 1 of this chapter assumed that no current flowed from the output of the network.
Where an output current flows, the timing is disturbed and the delay depends on the size of the current, which is not a desirable feature.
The solution is to 'buffer' the output of the **RC** network with a component such as a NOT gate. The output current then comes from the power supply to the NOT gate and not from the **RC** network itself. The **RC** network controls only when the NOT gate switches.

The circuit opposite shows a **RC** discharge circuit buffered by a NOT gate.
When switch **S** is momentarily closed, the capacitor charges to the supply voltage V_S, raising the NOT gate input to logic **1.**
As a result, the output of the NOT gate switches to logic **0**.
Once the switch is released, the capacitor begins to discharge and the voltage across it falls. Assuming that the NOT gate output changes when its input reaches ½ $V_{0,}$ this happens after 0.69 **RC** seconds.



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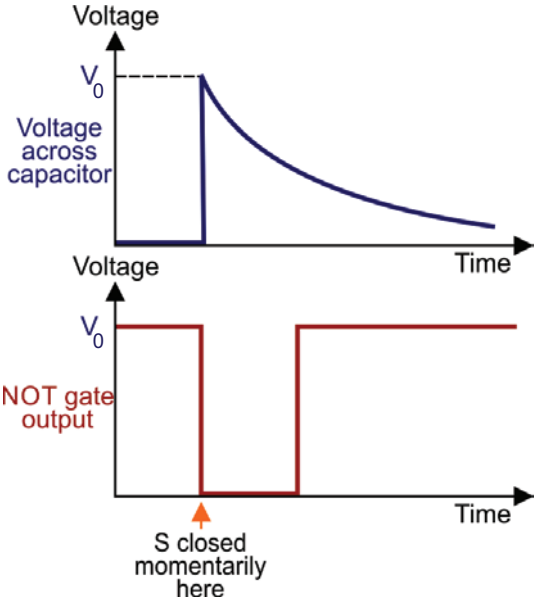
The output of the NOT gate stays low for 0.69 **RC** seconds and then returns to its stable high state until triggered again by pressing switch **S**.

This behaviour is illustrated in the graphs opposite.

Changing the resistor (or capacitor) value changes the delay (the time for which the NOT gate output sits at logic **0**).

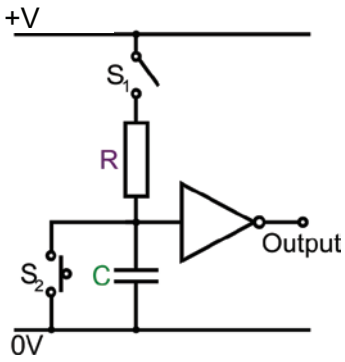


Now, consider the equivalent using the **RC** charging circuit.

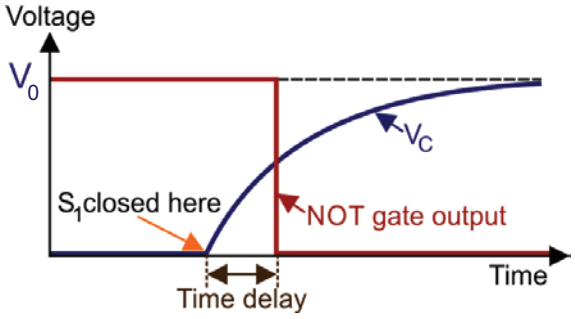
Initially, switch S_2 is pressed to discharge the capacitor, making the NOT gate input sit at logic **0** and its output at logic **1**.

When switch S_1 is closed, the capacitor charges up. As a result, the voltage at the input of the NOT gate rises and eventually reaches the logic **1** threshold.

At this point, the output of the NOT gate switches to logic **0**.

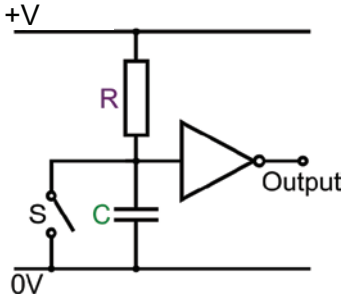


This behaviour is shown in the graph below.



There are practical issues with this circuit. It requires two switches, S_1, which has to be left closed long enough for the capacitor to charge, and S_2 which has to be momentarily closed before S_1 to initialise the circuit.

A modified version, using only one switch, is shown opposite. Switch **S** is normally closed. The input to the NOT gate sits at logic **0** and so its output will be logic **1**.
When switch **S** is opened, the capacitor charges and the voltage at the input of the NOT gate rises. When it reaches the logic **1** threshold, the output of the NOT gate switches to logic **0**.
The basic operation is the same. One issue is that the NOT gate and **RC** network remain 'powered up' unless the wider system includes a master 'power' switch elsewhere.



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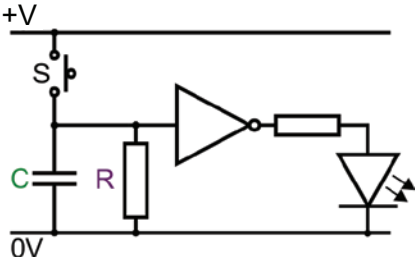
Designing monostable circuits

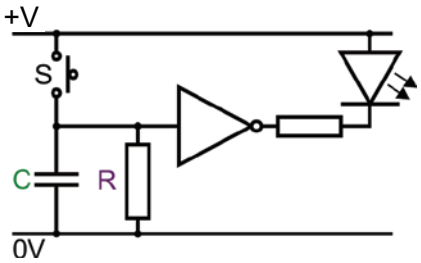
Monostables, using a **RC** network and NOT gate, provide an easy method of creating a delay.
However, remember that a monostable using the **RC charging** circuit needs a switch in parallel with the capacitor to discharge it.
So far we have not specified the required behaviour of the load attached to the monostable.

1. In this circuit, the LED lights when the NOT gate output is logic **1** – the NOT gate **sources** the current.



- In the stable state, the capacitor is discharged, making the NOT gate input logic **0** and its output logic **1**. The LED is lit.
- When switch **S** is pressed momentarily, the capacitor charges to V_0, changing the input of the NOT to logic **1** and its output to logic **0**. The LED turns off.
- The capacitor starts to discharge and after a time equal to 0.69 **RC**, the input of the NOT gate reverts to logic **0**. The NOT gate output changes to logic **1** and the LED switches on again.

2. In this circuit, the LED lights when the NOT gate output is logic **0** – the NOT gate **sinks** the current.



A similar argument shows that the LED is off initially. When **S** is closed, the LED turns on for time equal to 0.69 **RC**.

The CMOS 4049 inverting hex buffer contains six (hence ‘hex’) NOT gates. It is useful in these applications as the NOT gates switch when the input is approximately half of the supply voltage. It can source about 10 mA, sink over 40 mA and the input current is negligible.

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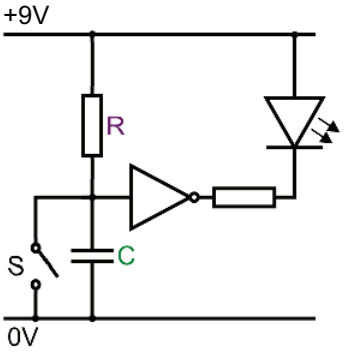
Example 1:

Design a circuit, using a 9 V power supply, which switches the LED on after a delay of approximately 20 seconds once switch **S** is opened.

The basic circuit is shown opposite.



Assuming that the output of the NOT gate changes when its input reaches ½ V_0, we select values of **R** and **C** which cause the voltage across the capacitor to fall to 4.5 V in 20 seconds.

In other words, we want a half-life, t, of approximately 20 seconds. Using the formula:

$$t = 0.69.\mathbf{R}.\mathbf{C}$$

$$20 = 0.69.\mathbf{R}.\mathbf{C}$$

so that:

$$\mathbf{R}.\mathbf{C} = \frac{20}{0.69}$$

$$= 28.99$$

Start by choosing the capacitor value, as normally the range of capacitor values is more restricted.

Try: **C** = 1000 µF

Then: **R** ≈ 29 kΩ

The nearest preferred value is 30 kΩ.

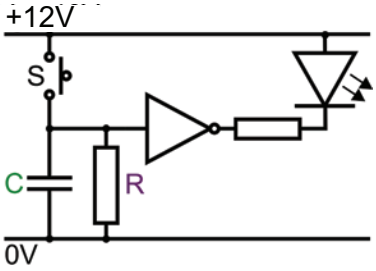
Using these values in the circuit diagram allows the monostable to be built and tested.

Where the delay period is critical, it is normal to use a variable resistor, allowing fine tuning of the time delay.

Example 2:

Design a circuit, using a 12 V power supply, that switches on an LED for approximately 10 seconds after switch **S** is momentarily pressed and released.

The basic circuit is shown opposite:



Assuming that the output of the NOT gate changes when its input voltage reaches ½ V_0, the values of **R** and **C** are chosen to give a half-life, t, of around 10 seconds.

Using:

$$t = 0.69.\mathbf{R}.\mathbf{C}$$

$$10 = 0.69.\mathbf{R}.\mathbf{C}$$

so that:

$$\mathbf{R}.\mathbf{C} = \frac{10}{0.69}$$

$$\approx 14.5$$

Using the same capacitor as before:

C = 1000 µF

Then: **R** ≈ 14.5 kΩ

The nearest preferred value is 15 kΩ.

Using these values in the circuit diagram allows this second monostable to be built and tested.

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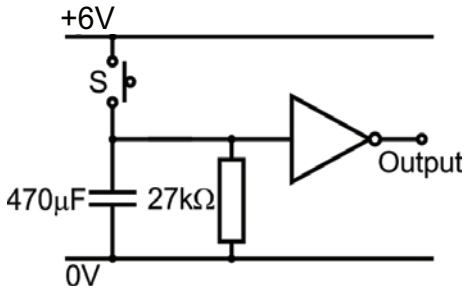
Example 3:

This time, the circuit for the monostable sub-system is provided. The task is to analyse it.

For the circuit shown, determine the time taken for the output to change after the switch is momentarily closed and then reopened.

(Assume that the output of the NOT gate changes when its input reaches 3 V.)



Using the assumption given in the question, the output of the NOT gate changes when its input reaches 3 V, which is half of the supply voltage. The time taken to do this is the half-life of the monostable.

Using: $t = 0.69.\mathbf{R}.\mathbf{C}$

$= 0.69 \times 27 \times 10^{3} \times 470 \times 10^{-6}$

so that: $= 8.76$ s

≈ 9 s

The delay between the switch being opened and the output changing will be roughly 9 s.

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Investigation 2.2

Note: If using 'Circuit Wizard':

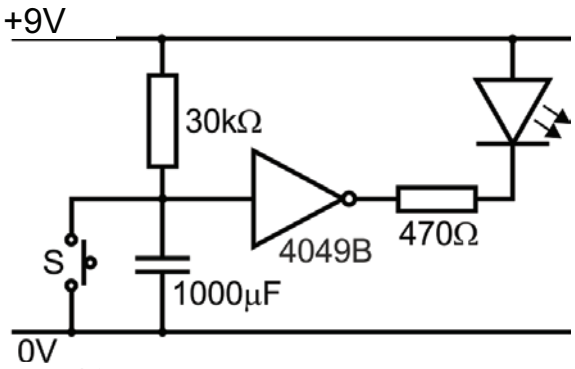
- ensure that you are taking readings in real time by going to:
  Project / Simulation / Timing Control
  and changing the *Time Base* to 1 s;

- ensure that voltage setting for the CMOS 4049 is set to power supply voltage by going to:
  Project / Simulation / Power Supply
  and checking the voltage setting.

A. Set up the circuit show on the right and close switch **S**.

Open switch **S** and use a stopwatch to measure the delay before the LED turns on.

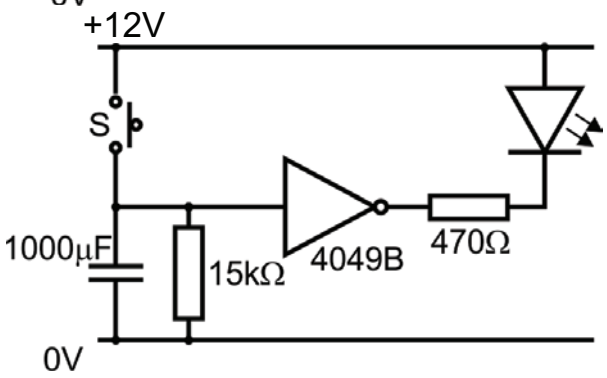
Time = ... s.



B. Set up the circuit show on the right.

Momentarily close switch **S** and use a stopwatch to measure how long the LED stays on.

Time = ... s.



C. Compare your results with the answers given in **Examples 1** and **2**.

Can you give reasons for any differences?

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Exercise 2.4

For all three questions, assume that the NOT gate output changes logic level when the input reaches half of the supply voltage

1. Design a monostable circuit using a **RC** network and NOT gate that switches on a LED for approximately 45 s after a switch is momentarily closed and released. It operates on a 12 V power supply.

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2. An alarm system is required to switch on a buzzer exactly 3 minutes after a safe door is opened. The circuit uses a **RC** network, a NOT gate and a component that allows the time to be adjusted to exactly 3 minutes. It operates on a 6 V power supply.

Draw your design in the space provided and show any calculations used to determine component values.

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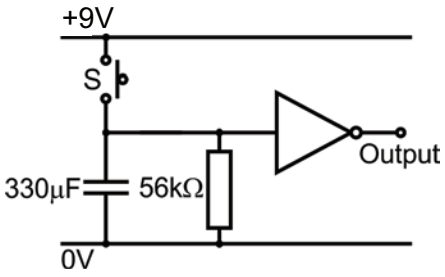
3. For the circuit shown, determine the time taken for the output to change after the switch is momentarily closed and then opened.



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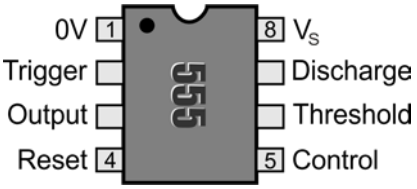
3. The 555 Timer IC

Introduction

The 555 timer is one of the most widely used ICs in electronics, at the heart of many astable, and monostable circuits.

The diagram shows the pinout for the usual format of the 555 timer IC, though you are not required to memorise it or the information that follows. Both will be useful when you use the IC in investigations and project work.



555 behaviour:

- pin 1: power supply connection to 0 V.
- pin 2: active low trigger – the timing starts (i.e. output voltage goes high,) when the voltage on this pin drops below one-third of the supply voltage.
- pin 3: output pin – the output voltage is either low (close to 0 V) or high (close to the power supply voltage).
- pin 4: active low reset pin – used to restart timing, when triggered again, if momentarily grounded.
- pin 5: control voltage pin – usually connected to 0 V through a small capacitor to filter minor power supply fluctuations.
- pin 6: threshold – the timing ends (i.e. output voltage goes low,) when the voltage on this pin reaches two-thirds of the supply voltage.
- pin 7: discharge – discharges the external timing capacitor.
- pin 8: connects to the positive power supply voltage (between 4.5 V and 15 V).

4. The 555 Monostable

Learning Objectives:

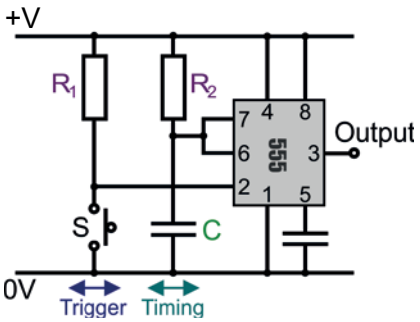
At the end of this topic you should be able to:

- draw the circuit diagram for a monostable using a 555 timer IC;
- calculate the time period for a 555 monostable circuit using the formula: T = 1.1 **RC**;
- design a 555 monostable to meet a given specification.

Here is the standard circuit diagram for a 555 monostable.
The time delay produced by it is given by the formula:

$$T = 1.1RC$$

(This equation is given with the examination paper and so need not be memorised. However, candidates are expected to recall and draw this circuit diagram for a 555 monostable.)



Notes :

- The minimum value of resistance for the timing resistor is 1 kΩ. Limiting the current in this way prevents overheating the component.
- The small capacitor connected to pin 5 is usually 10 nF – the precise value is unimportant for any calculations.

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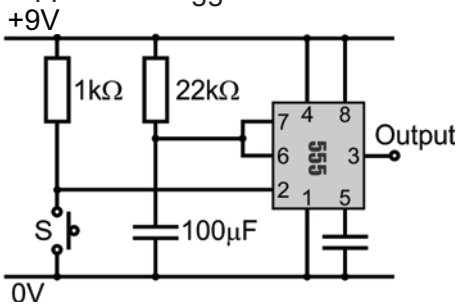
Example 1:

Calculate the time delay produced when the monostable circuit shown opposite is triggered.



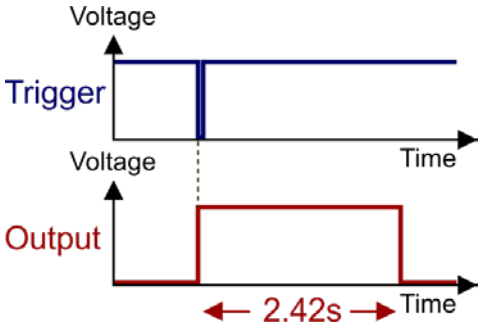
The time delay, **T**, produced by the monostable timer is:

$$T = 1.1\ R\ C.$$
$$= 1.1 \times 22 \times 10^{3} \times 100 \times 10^{-6}$$
$$= 2.42\ s$$

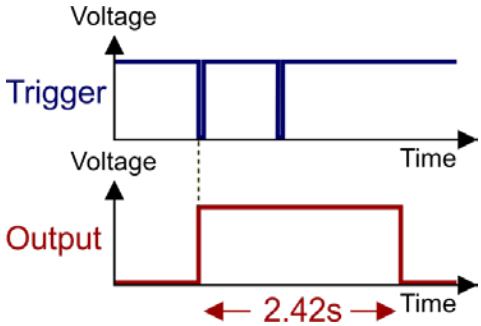
Features

The following graphs illustrate some features of the behaviour of this monostable circuit:

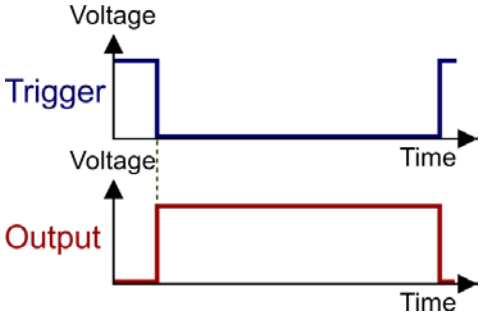
- When the trigger (pin 2) is pulled low by closing switch **S** the output goes high and stays there for the calculated period of 2.42 s.



- If a second trigger event occurs before the timing period has ended, this pulse is ignored.



- If the switch is held closed for too long, producing a very long trigger pulse, the output remains high beyond the normal duration.



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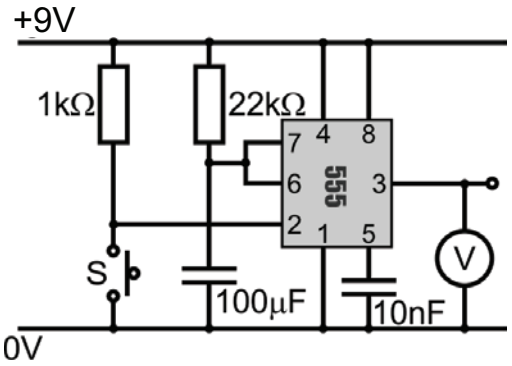
Investigation 2.3

Note: If you are setting this circuit up on 'Circuit Wizard' check that the simulation time base is set to 1 s and the voltage setting to 9 V.

a) Set up the circuit show opposite.



Momentarily close switch **S.**

Use a stopwatch to measure the time for which the output is 'high' (the voltmeter reading = 9 V).

Time = ... s.

Compare the result with the answer given in the **Example**.

.....
.....

b) What would you expect the monostable period to be if the 22 kΩ resistor were replaced by a 220 kΩ one?
.....

Modify the circuit by changing the resistor and measure the new period.

Period = ... s.

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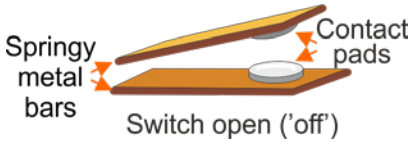
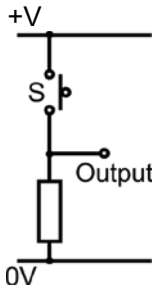
Switch Bounce

A switch is simply two metal bars, separated by air when switched ‘off’ and pressed into contact when ‘on’.



However, metal is ‘springy’ and when the metal bars flick into contact, they bounce off again and can do so a number of times.

When the switch is connected in series with a resistor, in a switch unit, as shown in the circuit diagram opposite, the effect is the same as if the user had closed and opened the switch several times rapidly.



The graph below shows the results of switch bounce on the output of a switch unit. In an electronic counter, for example, this switch bounce can cause the system to jump several counts for each switch press.

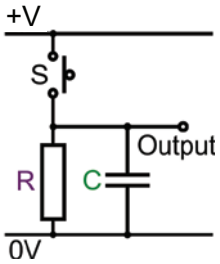
(This bouncing is usually finished within a few milliseconds.)

Curing switch bounce 1: Using a RC network

One approach to ‘debouncing’ the switch is to connect a capacitor in parallel with the resistor, creating the discharge circuit discussed earlier.

This approach relies on the fact that the voltage across a capacitor changes only slowly.

On first contact, the switch connects the capacitor to the positive supply rail and the capacitor charges rapidly to that voltage.



Further bounces of the switch contacts do little, as the capacitor has not had time to discharge much.

The overall effect is that the rest of the circuit does not ‘see’ the effects of the switch bounce.

This approach has limitations:

- if the time constant of the **RC** network is too large, the action of the circuit will slow, since the slow capacitor discharge renders the circuit insensitive to switch presses for some time;
- if the time constant of the **RC** network is too small, some of the switch bounces will not be suppressed.

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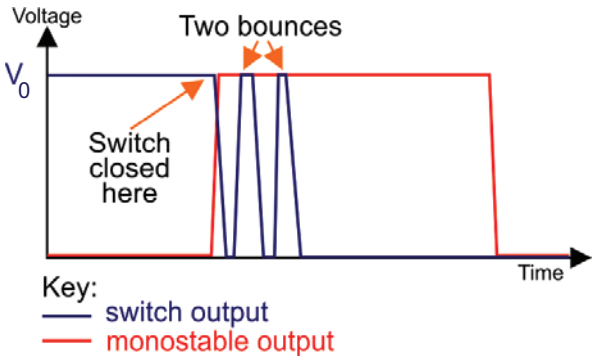
Curing switch bounce 2: Using a monostable

A better solution to the problem of switch bounce is to follow the switch unit with a monostable 'debouncing' circuit.

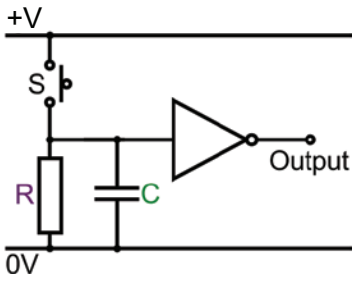
Monostable debounce circuits rely on the fact that further trigger pulses, occurring before the monostable 'times out', are ignored.



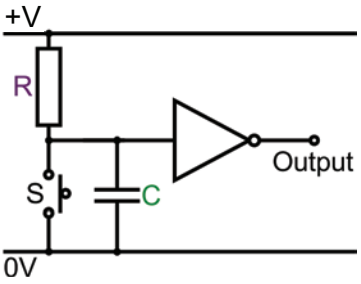
The graph opposite shows that the output pulse begins on the first trigger pulse. Additional trigger pulses occurring before the end of the monostable pulse are ignored.

An output pulse lasting ten milliseconds is usually sufficient to mask the switch bounce pulses.

Suitable monostable circuits for this application include the 555 monostable or one of the following simple buffered **RC** network monostables.



Pressing the switch produces a falling-edge pulse



Pressing the switch produces a rising-edge pulse

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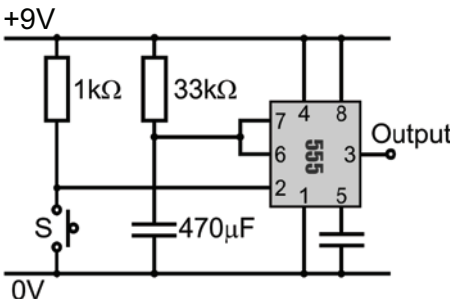
Exercise 2.5

1. The circuit diagram shows a 555 IC configured as a monostable timer.



Calculate the duration of the output pulse when the switch **S** is pressed momentarily.

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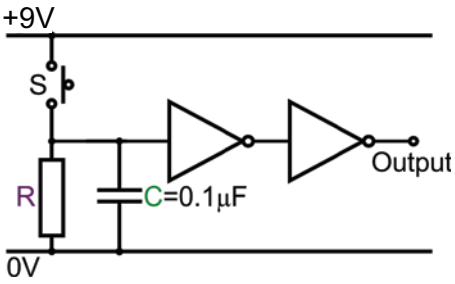
2. The following diagram shows a simple debounce circuit.



a) The circuit must generate a rising-edge output pulse of about 8 ms duration. The inverter outputs change logic level when the input voltage reaches 4.5 V. Determine the suitable preferred value for **R**.

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b) Why are two inverters needed for this circuit?

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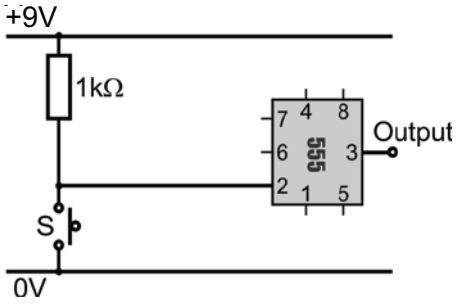
3. The diagram shows an incomplete circuit for a 555 monostable timer.



a) Complete the circuit diagram for the 555 monostable timer.

b) The circuit must produce a time delay of approximately 2 minutes.

Determine the value of all components that you have added.

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5. Astable Circuits

Learning Objectives:

At the end of this topic you should be able to:

- recall that an astable circuit has two unstable states;
- calculate the mark space ratio for an astable signal.

Introduction

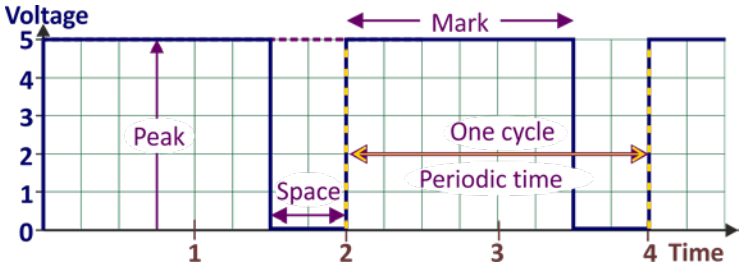
The astable circuit is used in a variety of applications, such as causing flashing lights and pulsing buzzers in alarm circuits and triggering counters.

Ideal astable behaviour

The previous section looked at the behaviour of monostable circuits, which had just one stable state. In contrast, the astable circuit has no stable states. Its output switches continually between logic **1** and logic **0**. It is sometimes known as a 'pulse generator' or a 'clock'.

The parameters of the signal generated by an astable circuit include the 'mark-space ratio'. The 'mark' refers to the 'on' time (at logic **1**), the 'space' is simply the 'off' time (at logic 0). For example, a mark-space ratio of 3:1 means that the 'on' time must be three times as long as the 'off' time.

The output of an astable circuit is shown in the timing diagram below. Logic **1** is represented by +5 V and logic **0** by 0 V in this diagram:



The peak voltage is also known as the amplitude of the signal.

For this signal:

- Peak voltage = 5 V
- Periodic time = 2 s
- Mark-space ratio = 3:1

As for all periodic signals, frequency $f = \frac{1}{T}$ where **T** is the periodic time (usually referred to as simply the **period**). In this case, then, frequency = $\frac{1}{2}$ = 0.5 Hz.

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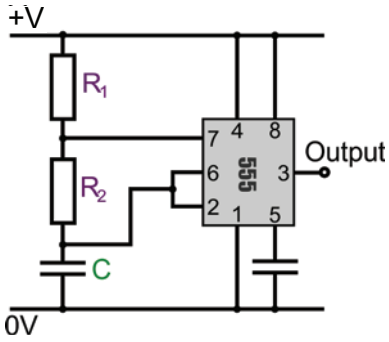
6. The 555 Astable

Learning Objectives

At the end of this topic you should be able to:

- draw the circuit diagram for an astable using a 555 timer IC;
- select and use the following formulae for a 555 astable circuit:
  - the time the output is high: $t_H = 0.7(R_1 + R_2).C$
  - the time the output is low: $t_L = 0.7R_2C$
  - the pulse frequency: $f = \frac{1.44}{(R_1 + 2R_2).C}$
  - mark:space ratio: $\frac{T_{ON}}{T_{OFF}} = \frac{R_1 + R_2}{R_2}$
- design a 555 astable to meet a given specification.

The circuit diagram for one form of 555 astable circuit is shown below.



(The examination requires that you are able to recall the circuit diagrams for both the 555 monostable timer and the 555 astable. It is important that you do not confuse the two.)

Four formulae apply to this astable circuit.
The formulae are:

- the time t_H for which the output is high (the mark): $t_H = 0.7(R_1 + R_2).C$
- the time t_L for which the output is low (the space): $t_L = 0.7R_2C$
- the frequency of the pulses produced: $f = \frac{1.44}{(R_1 + 2R_2).C}$
- mark:space ratio: $\frac{T_{ON}}{T_{OFF}} = \frac{R_1 + R_2}{R_2}$

Notes:

- The 'mark' is always longer than the 'space'. They are roughly the same if $R_2 >> R_1$.
- The minimum value of resistance for R_1 and R_2 is 1 k to prevent overheating.
- Once again, the capacitor on pin 5 is ≈ 10 nF but the actual value is unimportant.

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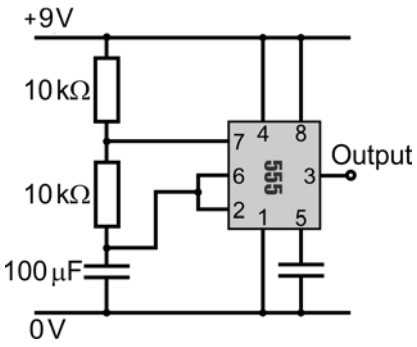
Example 1:



For the 555 astable shown opposite, calculate:

(a) the time t_H for which the output is high;
(b) the time t_L for which the output is low;
(c) the mark:space ratio;
(d) the frequency of the pulses produced.

(a) $t_H = 0.7(R_1 + R_2).C$
$= 0.7(10\times10^3+10\times10^3).100\times10^{-6}$
$= 1.4$ s

The output is high for 1.4 s.

(b) $t_L = 0.7R_2C$
$= 0.7\times10\times10^3\times100\times10^{-6}$
$= 0.7$ s

The output is low for 0.7 s.

(c) These results can be written as: Mark = 1.4 s Space = 0.7 s.
The mark:space ratio is therefore 2:1.

Alternatively,

$$\frac{T_{ON}}{T_{OFF}} = \frac{R_1 + R_2}{R_2}$$

$$\text{Mark: Space} = \frac{10\ \text{k}\Omega + 10\ \text{k}\Omega}{10\ \text{k}\Omega}$$

$= 2{:}1$

(d) $$f = \frac{1.44}{(R_1 + 2R_2).C}$$

$$= \frac{1.44}{(10\times10^3+20\times10^3).100\times10^{-6}}$$

$= 0.48$ Hz

The pulse frequency is 0.48 Hz.

Alternatively,

$$f = \frac{1}{t_H + t_L} = \frac{1}{2.1} = 0.476\ \text{Hz}$$

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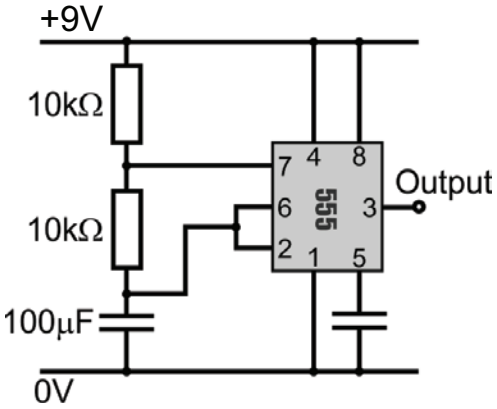
Investigation 2.4

You will need to use an oscilloscope for this investigation. Your teacher will show you how to use a real oscilloscope or the one provided on the simulation software.

Set up the 555 astable circuit shown opposite.



a) Use an oscilloscope to determine:

i) the time t_H for which the output is high;

t_H = ... s.

ii) the time t_L for which the output is low;

t_L = ... s.

iii) the period of the pulses produced.

period = ... s.

b) Now calculate the frequency of the pulses produced:

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frequency = ... Hz.

c) Compare these answers with those given in the **Example**:

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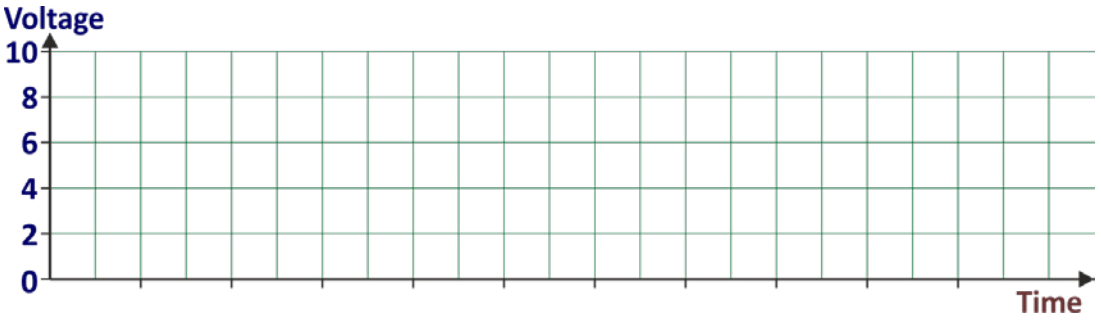
d) Sketch the output signal on the graph grid below.
The graph should show two cycles of the waveform. Label the time axis clearly.



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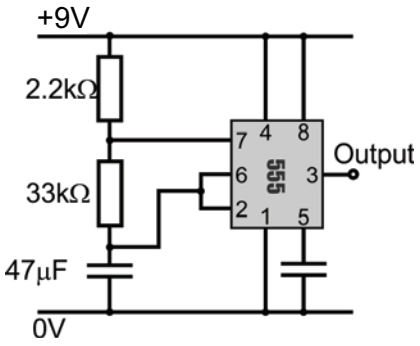
Exercise 2.6

1. For the 555 astable circuit shown opposite, calculate:



a) the time t_H for which the output is high;

b) the time t_L for which the output is low;

c) the mark:space ratio;

d) the frequency of the pulses produced.

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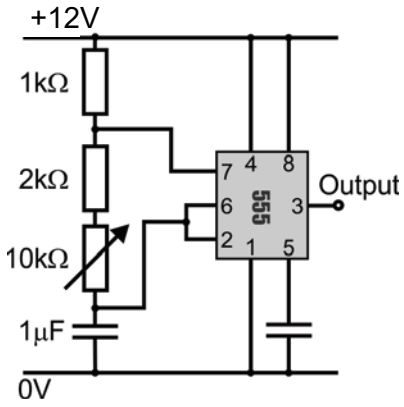
2. The 555 astable circuit shown opposite controls the speed of a motor by switching on and off rapidly. Adjusting the variable resistor changes the length of time for which the motor is on (the 'mark'.)



For this circuit, calculate the maximum and minimum values of:

a) mark:space ratio;

b) frequency.

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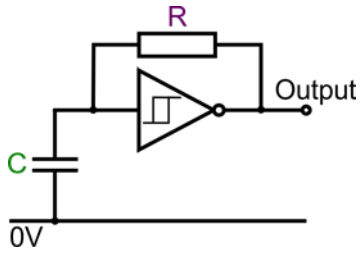
7. The Schmitt Inverter Astable

Learning Objectives

At the end of this topic you should be able to:

- explain the operation of an astable, based on a Schmitt inverter, and estimate the operating frequency using: $f \approx \frac{1}{R.C}$
- design an astable, based on a Schmitt inverter, to meet a given specification.

One way to create an astable sub-system is to use a Schmitt inverter. The circuit diagram is shown below.



This is a simple circuit, but reliable and compact because of the small number of components involved.

The frequency of the output is given by the approximation: $f \approx \frac{1}{R.C}$

Note: The minimum value of resistance in this circuit should be 1 kΩ to limit the current and hence prevent the Schmitt inverter from overheating.

How does it work?

- Assume that the capacitor is uncharged initially, so that the input to the Schmitt NOT gate will be logic **0**. This means that the output is initially logic **1**.
- Capacitor **C** begins to charge through the resistor **R** and the voltage at the input of the Schmitt NOT gate starts to rise.
- When it reaches the upper switching threshold for the Schmitt inverter, its output changes to logic **0**.
- The capacitor now starts to discharge through **R** and the voltage across **C** falls.
- When this voltage reaches the lower switching threshold, the output of the Schmitt inverter changes to logic 1 again.
- Capacitor **C** starts to charge through **R** again and the whole process repeats.
- This continues as long as the power is switched on.

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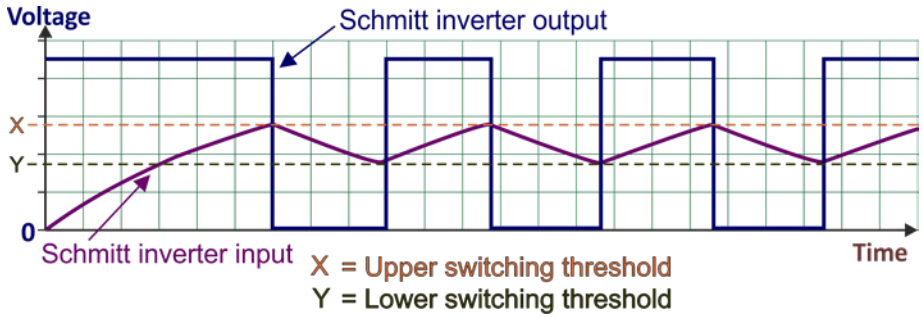
This behaviour is shown in the following graph.



Note:

- The first cycle lasts longer than subsequent pulses as the capacitor has to charge from 0 V (not the lower switching threshold) to the upper switching threshold.
- After the first cycle the capacitor charges and discharges between the upper and lower switching thresholds of the Schmitt NOT gate.
- The 'on' time, and 'off' time are of the same duration. In other words, the mark:space ratio is 1:1 and cannot be adjusted.
- The output current is very limited. Where the output current is significant, a buffer must be added.

Example 1:

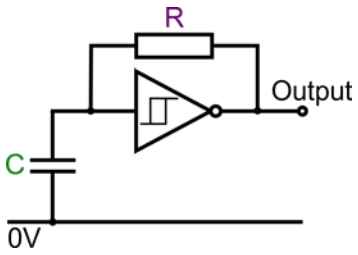
Design an astable circuit using a Schmitt Inverter to generate a signal with a frequency of 200 Hz.

Using the formula: $f \approx \frac{1}{R.C}$ gives a time constant **RC** of $\frac{1}{200}$ = 5 ms (= 5×10^{-3} s).

There is no single solution to this.

The table lists some of the **RC** combinations that could be used:

Resistor R	Capacitor C	Time constant RC
5.1 kΩ	1.0 μF	5.10 ms
15 kΩ	0.33 μF	4.95 ms
75 kΩ	68 nF	5.10 ms
330 kΩ	15 nF	4.95 ms



Some factors that can affect final choice are:

- leakage current of the capacitor – large value resistors may not pass sufficient current to charge up the capacitor to a sufficient voltage;
- low value resistors may demand too much current – the Schmitt inverter may not be able to deliver sufficient current / the resistor or inverter may overheat;
- physical size of the capacitor for the intended application;
- availability of components.

In this case, the best choice is probably **R** = 15 kΩ, and **C** = 0.33 μF.

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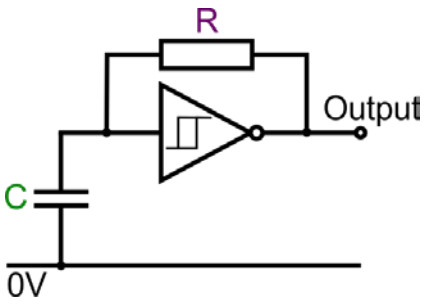
Investigation 2.5



Build the astable shown opposite.

Use a CMOS 40106 Schmitt Inverter and values:

- **R** = 15 kΩ;
- **C** = 0.33 µF.

Set the power supply voltage to 9 V.

a) Use an oscilloscope to measure the period of the pulses produced.

Period = ... s.

b) Now calculate the frequency of the pulses produced:

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frequency = ... Hz.

c) Compare your answer with that given in the **example calculation**:

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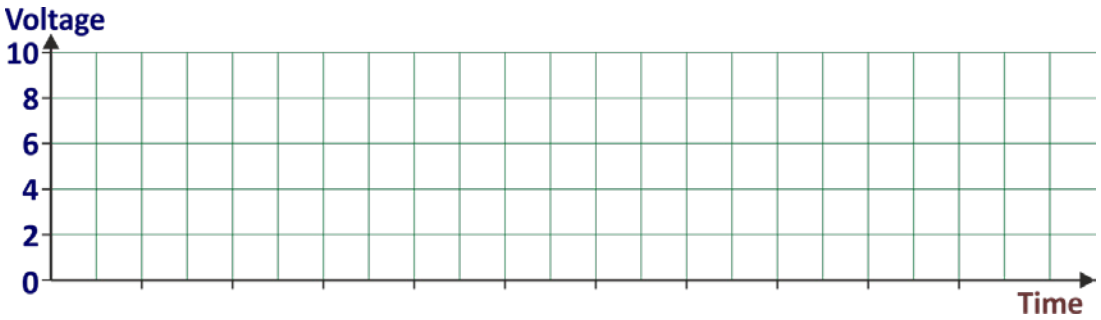
d) Sketch the output signal on the graph grid below.
The graph should show two cycles of the waveform. Label the time axis clearly.



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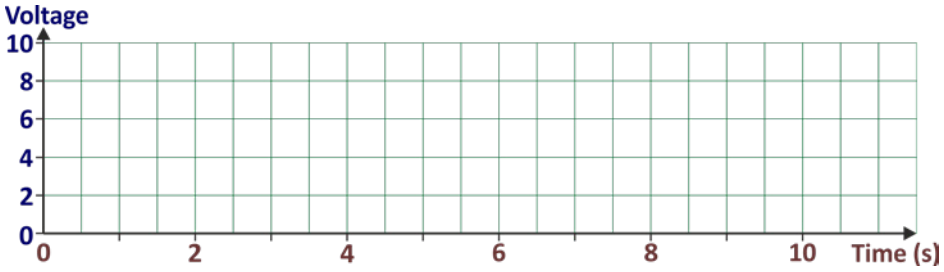
Exercise 2.7

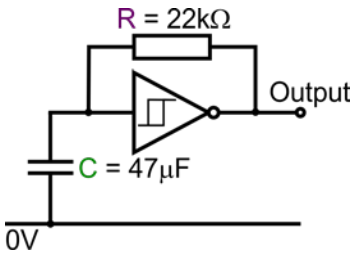
1. Use the grid below to draw an astable waveform with:

- peak voltage of 8 V;
- periodic time of 3 s;
- mark:space ratio of 2:1.



2. The astable circuit shown opposite has been pulsing for some time.

Calculate the frequency of the output signal produced



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3. Design an astable circuit using a Schmitt NOT gate which generates an output frequency of 2 Hz and operates on a 12 V power supply.

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